Chapter 1

Si, SiGe, and Si$_{1-y}$C$_y$ on Si: Epitaxy of Group-IV Semiconductors for Nanoelectronics

J. M. Hartmann
Université Grenoble Alpes and CEA, LETI, Minatec Campus, 17, Rue des Martyrs 38054 Grenoble Cedex 9, France


1.1. Introduction

Group-IV epitaxy is nowadays considered as a key enabler in Complementary Metal Oxyde Semiconductor (CMOS) devices, Bipolar and BiCMOS transistors, near infra-red photo-detectors or mid infra-red waveguides and so on [BAU 11], [WAD 15]. It is used in nanoelectronics for the fabrication of stressors (e.g. in-situ boron-doped SiGe and in-situ phosphorous-doped SiC recessed or raised sources and drains in short gate length devices), SiGe channels and so on, as shown in Figure 1 (see Refs. [HAS 14], [Liu 14] and references therein).

In the majority of these applications, epitaxy has to be selective on patterned wafers, e.g. without any deposition on dielectrics that surround Si (or SiGe) planar areas or fin-like structures. It is integrated in very complex
process flows, sometimes with severe thermal budget constraints, notably within the CoolCube™ integration scheme. In addition, growth occurs in very small areas (10–40 nm), often with significant thicknesses (8–30 nm). The vertical to horizontal aspect ratio then becomes an important process parameter. As current devices make full use of the third dimension, with fins or trigate structures instead of planar, bulk channels, growth will occur simultaneously on various surface orientations, leading to the appearance of facets and of variable thickness and composition films.

In the coming sections, we will first of all define what epitaxy is and introduce some important concepts such as critical thickness for plastic relaxation and so on. We will then move over to surface preparation prior to epitaxy, which is crucial when performing Selective Epitaxial Growth (SEG) on patterned wafers. The in-situ H₂ bake temperature (that follows a “HF-Last” wet cleaning) indeed needs to be lowered in order to avoid thin film islanding and/or shape change; innovative surface preparation schemes have then to be used in order to obtain high crystalline
quality epitaxial layers. We will subsequently detail some of the challenges one faces when growing on patterned wafers Si and SiGe layers with a chlorinated chemistry. We will notably cover the impact precursor mass-flows, temperature, substrate orientation, buried oxide thickness, mask opening and so on have on the Si and SiGe growth kinetics. We will then show how Si and SiGe(:B) SEG enabled us to obtain high performance p-type Field Effect Transistors on Extra-Thin Silicon-On-Insulator (ET-SOI) substrates and Si trigate structures. Finally, we will present the salient features of SiC:P and SiGe:B Cyclic Deposition/Etch (CDE) processes, which are very promising for low temperature epitaxy.

1.2. A few ideas about epitaxy

We will first of all explain what epitaxy stands for. To perform an epitaxy is to deposit a single-crystalline layer that will adopt the same crystalline structure as the single-crystalline substrate on which it is deposited, that is, a structure dictated by the underlying substrate. It is a homo-epitaxy when the substrate and the layer are of the same type (for example: Si on Si) and a hetero-epitaxy when they are not (for instance: SiGe on Si).

A layer is in tension (compression) when its lattice parameter $a_L$ is lower (higher) than that of the substrate $a_S$. For a pseudomorphic layer, the in-plane lattice parameter of the layer is equal to that of the substrate (i.e. $a_L^\parallel = a_S$). For a layer in tension, we then have $a_L^\perp < a_L < a_L^\parallel = a_S$; for one in compression, $a_L^\perp > a_L > a_L^\parallel = a_S$. The perpendicular lattice parameter is given (in cubic layers grown on (001) surfaces) by $a_L^\perp = a_L + 2c_{12}/c_{11}(a_L - a_S)$ (with $2c_{12}/c_{11}(\text{Si}) = 0.77$, $2c_{12}/c_{11}(\text{Ge}) = 0.74$ and $2c_{12}/c_{11}(\text{C}) = 0.61$).

Intrinsic or in-situ doped Si/SiGeC stacks (known as hetero-structures) are most of the time grown on Si substrates with a (001) surface orientation. Those substrates can be bulk-type or not (presence then of a buried oxide layer), blanket or patterned and so on. Let us summarize the main characteristics of the elementary compounds of a SiGeC alloy: Si, Ge and C crystallize in the diamond phase, i.e. two overlapping sphalerite structures shifted one from the other by a quarter of the large diagonal (cf. Figure 2).

The lattice parameter of C (i.e. the length of one of the sides of the cubes in Figure 1) is much smaller than that of Si, which in itself is smaller than that of Ge ($a_C = 3.567 \text{ Å} \Leftrightarrow a_{\text{Si}} = 5.43105 \text{ Å} \Leftrightarrow a_{\text{Ge}} = 5.65785 \text{ Å}$). The lattice parameter increase is accompanied by a sharp energy bandgap decrease: $E_g (\text{C}) = 5.48 \text{ eV} \Leftrightarrow E_g (\text{Si}) = 1.11 \text{ eV} \Leftrightarrow E_g (\text{Ge}) = 0.66 \text{ eV}$. Mixing Si, Ge and C in a SiGeC alloy will induce strong bandgap modifications; built-in stress will also play a role. Incorporating C by substitution into a Si or Ge matrix
Fig. 2. Schematics of the diamond structure of group-IV semiconductors and some of the surfaces on which growth will occur when processing 3D objects such as fins or tri-gates. The tetra-coordinated atoms are symbolized by light or dark grey spheres, while bonds appear as elongated cylinders.

is otherwise quite difficult. The miscibility of C in Si is only approximately $10^{-4}$ % at thermodynamic equilibrium (i.e. at 1400°C), with an unfortunate tendency towards SiC precipitate formation for high concentrations. Si and Ge, however, are miscible in all proportions. During hetero-epitaxy, there will be discrepancies between the lattice parameters of the deposited layer and the substrate, which will lead to an accumulation of elastic energy in the layer. For thin layers, the substrate’s atomic columns will be extended into the pseudomorphic epitaxial layer.

However, when the thickness of the layer increases, it becomes energetically favorable to introduce misfit dislocations to minimize the elastic energy that has accumulated and accommodate the lattice parameter mismatch between the layer and the substrate. The layer is then said to be plastically relaxed. The thickness at which the transition from pseudomorphic to plastically relaxed layer occurs is called critical thickness for plastic relaxation. Schematic diagrams in Figure 3 show the different configurations of the {epitaxial SiGe layer on Si substrate} system.

We have recently revisited the critical thickness for plastic relaxation of SiGe on Si(100). For this, 200 mm Si substrates (of a higher crystalline quality than those used in studies referenced in [HOU 91], i.e. with a lower pre-existing dislocation density) were used as templates for the Reduced Pressure — Chemical Vapor Deposition (RP-CVD) of variable composition and thickness SiGe layers.

The growth temperature was reduced from 700°C to 650°C, then to 600°C and finally to 550°C as the Ge concentration increased from 12% to 52% in order to reduce surface roughness. Due to differences between Molecular Beam Epitaxy (MBE) and RP-CVD in terms of Si and Ge precursors (solid ingots of Si and Ge which are sublimated by MBE $\leftrightarrow$ ultrapure gaseous precursors for CVD), the way very low partial pressures of
impurities such as oxygen or water are obtained (ultrahigh vacuum in MBE ⇔ large fluxes of ultra-pure hydrogen in CVD) and so on, we expect differences between [BEA 84, HOU 91, HAR 11a] findings. Figure 4 shows the summary of the results [HAR 11a]. The dotted line shows those of Bean [BEA 84], the full squares correspond to SiGe layers seen as fully compressively-strained in X-ray Diffraction or XRD and the squares with a cross in their center represent partially relaxed SiGe layers. $h_c$ is in fact two to three times higher than predicted by People and Bean. However, for high Ge concentrations, some layers seen as pseudomorphic in XRD are actually characterized by the presence of a limited amount of misfit dislocations in their midst. The surface signature of their propagation (“plough” lines along the $\langle 110 \rangle$ crystallographic directions) was detected thanks to Atomic Force Microscopy (hatched zone in Figure 4).

1.3. Surface preparation prior to epitaxy

The substrate surface preparation before any epitaxy is of prime importance. The goal is indeed to duplicate the atomic columns of the substrate into the layer. The presence on the surface of amorphous silicon oxide layers (even very thin ones), polymers or etching residues (on masked substrates) has indeed a crippling effect on the epitaxy quality. Depending on the toolset available for surface preparation and the nature of the substrate itself, three strategies may be used to obtain contamination-free Si (or SiGe) surfaces.

The starting substrate may be bulk Si or, to a lesser degree, a Silicon-On-Insulator — type substrate (i.e. a thin layer of Si/ buried layer
of SiO₂/Si substrate) stack, usually fabricated using the Smart Cut™ technique [BRU 95]). It is then possible to carry out high temperature bakes, during which dozens of liters of ultra-pure H₂ (typically only a few parts per billion of impurities thanks to dedicated gas purifiers) are injected into the epitaxy chamber, in order to remove the 0.8-1 nm thick layer of native or chemical SiO₂ which is initially present on the surface and smooth it. The simplified chemical reaction for the removal of the oxide layer is:

\[
\text{SiO}_2(s) + 2\text{H}_2(g) \rightarrow \text{Si}(s) + 2\text{H}_2\text{O}(g)
\]

The need for high thermal budgets (typically higher than 1050°C for 1 minute; 1100°C for 2 minutes as the CEA-LETI standard) prohibits the use of this surface preparation on patterned wafers (i.e. with active Si zones surrounded by dielectrics) or ion implanted substrates. The active zones could facet due to strain generated by masking dielectrics, especially if they are in a Shallow Trench Isolation (or STI) configuration. An exo-diffusion of pre-implanted atoms and a consequent auto-doping of the epitaxial layer may also take place [CHA 85, JER 99]. This type of bake is prohibited for thin Si films (e.g. less than 20 nm) on top of buried oxides. If these criteria are not respected, moat recess and islanding of the films will take place [ISH 99]. It is also wise to optimize the power delivered to the lamps used to heat up the

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**Fig. 4.** Critical thickness for plastic relaxation in Si₁₋ₓGeₓ epitaxial layers on Si (001) versus the Ge concentration x [HAR 11a]. 200 mm data.
SOI substrates so that the temperature at the surface is uniform; otherwise slip lines will form.

The surface preparation described above (where a native or chemical oxide present at the surface is removed by an in-situ H$_2$ bake in suitable conditions) is far from being universal given the high thermal budgets needed. In order to minimize the latter, the following sequence is then typically used:

(i) The native SiO$_2$ oxide is removed by a “HF-Last” wet cleaning [ABB 04]. During the next to last step of such a cleaning, the wafer is dipped in hydrofluoric acid diluted in deionized and de-oxygenated water (dilution typically between 0.2% and 1%), to etch surface SiO$_2$. The dissolution reaction is as follows:

$$\text{SiO}_2 + 4\text{HF} \rightarrow 2\text{H}^+ + \text{SiF}_6^{2-} + 2\text{H}_2\text{O} \quad \text{[BUH97]}$$

The etch rate of thermal SiO$_2$ (the most resistant of all) is of the order of 1.2 to 1.4 nm min$^{-1}$ for 0.2% HF. During the last step, the wafer is rinsed in deionized and deoxygenated water to remove all traces of HF. The wafer is then dried by for instance isopropyl alcohol vapors, before being loaded as quickly as possible in the load-lock chambers of the epitaxy tool, in an inert atmosphere (purified N$_2$). After such a wet cleaning, approximately 85% of the Si dangling bonds are occupied by hydrogen atoms. The remaining 15% are mainly occupied by fluorine atoms as well as oxygen and carbon contaminants [MEY 90, TRU 90].

(ii) An H$_2$ in-situ bake then takes place at temperatures above 800$^\circ$C to remove all O, F or C surface contaminants (if compatible with the technology it will be used in). A surface perfectly passivated by hydrogen atoms is then obtained which is ideal for epitaxy.

An “HF-last” surface is only stable for a few dozens of minutes up to a couple of hours (before the re-growth of a native oxide a few Å thick can be detected by spectroscopic ellipsometry). Minimizing the time between a “HF-Last” wet cleaning and the loading of wafers inside chambers purged with high purity inert gases (such as N$_2$) is thus mandatory [WOS 14a]. A perfectly hydrogen-passivated Si surface obtained by a high temperature H$_2$ bake is by contrast stable for several days [HER 01].

We will now focus on the impact of the H$_2$ bake temperature on the properties of the epitaxial layers and the interfacial contamination, this for Si, SiGe and pure Ge surfaces of (100) and (110) crystallographic orientations.
We have plotted in Figure 5 the surface haze values associated with 100 nm thick Si layers grown with SiH$_4$ at 700°C, 80 Torr in LETI’s 300 mm ASM Epsilon 3200 Epsilon epitaxy tool after the following surface preparation of the Si(001) substrates: (i) a “HF-Last” wet cleaning in a state-of-the-art DNS 3100 single wafer cleaning tool followed by (ii) an in-situ H$_2$ bake at 80 Torr for 225s at various temperatures: 750°C, 775°C, 800°C, 825°C and 850°C. Be it in the Dark Wide or Dark Narrow configuration of the SP2 metrology tool, we are faced with a very significant decrease of the haze (e.g. the light diffusion by the surface, which is proportional to the surface roughness [HAR 11a]) as soon as the bake temperature exceeds 775°C. Haze after 825°C–850°C bakes is indeed nearly 50 times lower than haze after 750°C–775°C H$_2$ bakes; it is close to values expected after a perfect Si epitaxy.

We have plotted in Figure 6 the interfacial O, C and F contamination (from Secondary Ion Mass Spectrometry) as a function of the H$_2$ bake temperatures in those samples. Be it at 825°C or 850°C, we are contamination-free (e.g. below the SIMS lower limits of detection of the elements probed: $10^{11}$ cm$^{-2}$ for O and C $\leftrightarrow 5 \times 10^9$ cm$^{-2}$ for F). By contrast, we are faced with a significant interfacial C, O and F contamination at 750°C and 775°C, with notably an oxygen sheet concentration a third of the Si surface concentration ($2.4 \leftrightarrow 6.8 \times 10^{14}$ cm$^{-2}$).
The situation is intermediary at 800°C, with O and F interfacial concentration several orders of magnitude lower than at 750°C and 775°C. The excellent correlation between Figure 5 haze evolution and Figure 6 interfacial contamination is to be highlighted.

SIMS has been used a while ago to profile the C, O and F atoms present in 50 nm thick Si layers grown at 650°C on Si (001) substrates (in LETI’s 200 mm AMAT Epi Centura 5200 epitaxy tool) after a “HF-Last” wet cleaning followed by a two minutes, 20 Torr H₂ bake, either at 750°C or 775°C [ABB 04]. 750°C was too low to get rid of F and O contamination. Peaks were indeed present at the interface between the substrate and the epitaxial layer. No such peaks were observed at 775°C, however (same findings in [KOR 08]). These results are in full agreement with those of Brabant, who showed that 750°C H₂ bakes lasting as long as 10 to 20 minutes did not completely rid the Si(001) surface from O contamination [BRA 03]. Interfacial O contamination disappeared after 800°C H₂ bakes in [WOS 14b].

It is interesting to note that the H₂ bake threshold temperature around 775°C–800°C, above which C, O and F surface contamination is eliminated, does not seem to be influenced by the crystallographic orientation of the Si surface. A low interfacial O peak was shown by Destefanis [DES 08] after 20 Torr H₂ bakes at 775°C for two minutes (after “HF-Last” cleaning) of Si(110) substrates. This peak disappeared entirely at 800°C.
Similarly, changing, for (001) surfaces, from Si to SiGe or even pure Ge has little impact on the threshold temperature. O and F contamination peaks were indeed evidenced by Abbadie et al. [ABB 04] after 20 Torr H₂ bakes at 775°C for two minutes (post “HF-Last” cleaning) of SiGe 20% and 33% Strain Relaxed Buffers (SRBs) prior to their encapsulation with thin, tensily-strained Si layers. These contamination peaks disappeared at 800°C. With regards to pure Ge, there was no interfacial contamination peaks anymore after 20 Torr H₂ bakes at 750°C for two minutes [HAR 04a]; there was, however, a low O peak after bake at 700°C.

The H₂ bake pressure itself has also a definite impact on interfacial contamination; the higher it is, the lower the O removal efficiency will notably be. Hykavyy et al. were indeed faced, at 750°C, with a monotonous increase of the integrated O dose (at Si/Si interfaces) from $\sim 10^{13}$ atoms/cm² up to $\sim 7 \times 10^{13}$ cm⁻² when the bake pressure increased from 1 Torr up to 150 Torr [HYK 16]. At 800°C, the integrated O dose increased from $\sim 5 \times 10^{12}$ cm⁻² up to $\sim 3 \times 10^{13}$ cm⁻² when switching from 20 to 150 Torr. Such findings are fully in line with those shown in Figure 5, where the threshold temperature mandatory to get rid of interfacial contamination is roughly 50°C higher at 80 Torr than at 20 Torr.

The temptation would then be, given those data, to carry out the H₂ bake at high temperatures (typically between 850°C and 900°C) and low pressures (20 Torr and less) for relatively long durations (two minutes or more), in order to be safe. This is however not always possible.

On ultra-thin SOI substrates with a mesa isolation, there is for instance a moat recess at the edges of the active Si zones and possibly an islanding of the Si film if the thermal budget of the in-situ H₂ bake is too high (top left image of Figure 7). The H₂ bake is then typically carried out at 650°C, 20 Torr for two minutes prior to the selective epitaxial growth of Si raised sources and drains on ultra-thin SOI (i.e. with a starting Si layer thickness of 3 nm, typically) [JAH 05].

Too high a H₂ bake temperature may also lead, for MOSFET transistors with etched gates, to a detrimental regrowth of the interfacial oxide layer present between the Si channel and the high permittivity gate dielectrics (such as HfO₂) or a detrimental diffusion of ions which had previously been implanted to dope the extensions. Because of re-flow, Si nanowires will change shape, with squared-based sections becoming circular (bottom left images of Figure 7) [TAC 09] and the contacts with the sources and drains’ blocks becoming pinched-off and ultimately broken (right images of Figure 7) [DOR 07].
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Fig. 7. (top left) top-view SEM image of a 8 nm thick patterned SOI(001) film after a 950°C, 2 min. H$_2$ bake: moat recess and islanding; (bottom left) cross-sectional TEM images of rectangular Si NWs becoming circular after 750°C, 2 min. H$_2$ bakes. (right) top-view SEM images of suspended Si NWs after various temperature H$_2$ bakes lasting 2 minutes at 20 Torr: pinch-off then breaking-off at the contact regions with the source/drain pads. 200 mm data. [JAH 05], [DOR 07], [TAC 09].

What about the structural and electronic properties of the epitaxial layers on partially contaminated Si surfaces? The impact of too low a H$_2$ bake temperature (between 650°C and 750°C) to remove all traces of O, C or F contamination at the interface is limited on (001) surfaces. The surface stays smooth after epitaxy [DES 08], Si/SiGe/Si stacks are of high crystalline quality in X-ray Diffraction, the electrical performances of Fully Depleted transistors built on top of SOI or SiGe/Si dual channels [LER 11] with Si [AND 07] or SiGe:B [BAU 10] raised sources and drains are excellent and so on. However, H$_2$ bakes at too low temperature (i.e. T < 775°C for two minutes at 20 Torr) have a catastrophic impact on the crystalline quality of epitaxial Si layers grown on Si(110) substrates [DES 08].

Whatever the surface, specific care must be taken during lithography and etch steps to remove all polymers, High-K dielectrics residues (e.g. oxides from transistor gates) and so on. Failure to do so delays growth, prevents epitaxy from taking place if the H$_2$ bake temperature is too low.
and so on [HAR 11b]. It may even lead to a significant deterioration of the layer crystalline quality [Liu 12].

Dry plasma etching based on NH₃, NF₃ and H₂ gases in a “Siconi” chamber connected to an epitaxy cluster tool can also be used in order to get rid at low temperature of native oxyde. Chemical reactions are then as follows [YAN 10]:

(i) Etchants are generated in a remote plasma cavity:

\[
\text{NF}_3 + \text{NH}_3 \rightarrow \text{NH}_4\text{F} + \text{NH}_4\text{F} . \text{HF} \quad (1)
\]

(ii) SiO₂ is transformed at \(\sim 30^\circ\text{C}\) into a salt:

\[
\text{NH}_4\text{F} \quad \text{or} \quad \text{NH}_4\text{F} . \text{HF} + \text{SiO}_2 \rightarrow (\text{NH}_4\text{F})_2\text{SiF}_6 \text{ (solid)} + \text{H}_2\text{O} \quad (2)
\]

(iii) This salt is sublimated at low temperature (100°C < T < 200°C)

\[
(\text{NH}_4\text{F})_2\text{SiF}_6 \text{ (solid)} \rightarrow \text{SiF}_4 \text{ (gas)} + 2\text{NH}_3 \text{ (gas)} + 2\text{HF} \text{ (gas)} \quad (3)
\]

Surfaces stay pristine afterwards as wafers are transferred under ultra-pure nitrogen from the “Siconi” chamber to the epitaxy chamber itself. Interfacial contamination after wet cleaning in single wafer tools is then avoided. Indeed, 300 mm wafers do not stay any more in Front Opening Unified Pods (FOUPs) before being loaded into inert gases load-locks.

Combinations of dry plasma and wet cleaning can be very useful in order to get rid of deleterious “residues” on patterned wafers. We have provided in Figure 8 some 3D Scanning Electron Microscopy (SEM) images of transistors after the use of a 650°C, 120s + 750°C, 30s hybrid H₂ bake followed by the 650°C selective epitaxy of 18 nm thick Si₀.₇Ge₀.₃:B raised sources and drains on each side of the gate (everything at 20 Torr). 4 different \textit{ex-situ} surface preparation schemes were used beforehand:

(i) A “HF-Last” wet cleaning only;
(ii) The creation inside a remote “Siconi” chamber of the salt (e.g. reactions (1) and (2) above), this salt being sublimated afterwards in the epitaxy chamber;
(iii) A “HF-Last” wet cleaning followed by the creation inside a remote “Siconi” chamber of the salt (e.g. reactions (1) and (2) above), this salt being sublimated afterwards in the epitaxy chamber;
(iv) The full “Siconi” process (e.g. reactions (1) to (3)) followed by a “HF-Last” wet cleaning.
While “HF-Last” wet cleanings or “Siconi” processes are not by themselves enough to get rid of “residues” (presence after SiGe:B SEG of numerous holes in the S/D regions, especially with a “HF-Last” wet cleaning), we do see that combining them yields 2D layers [Lu 16].

1.4. Selective epitaxial growth of Si and SiGe with standard gaseous precursors

Dichlorosilane (SiH$_2$Cl$_2$) is the silicon precursor of choice for the Selective Epitaxial Growth (SEG) of Si and SiGe in the Si windows of patterned Si substrates, the masking layers being dielectrics such as SiO$_2$ or SiN. This Si
The growth rate of Si at 20 Torr is shown in Figure 9 as a function of the reverse absolute temperature for three surface orientations: (100), (110) and (111) [HAR 06]. The first two correspond to the top and sidewalls of fins, respectively, while the third one might occur when facets form.

There is as expected an exponential increase of the Si growth rate with the temperature. We have extracted from those Arrhenius plots the activation energies associated with the (100), (110) and (111) surface orientations. They slightly increase with the Miller indexes of the surface: \( E_a \) \( \text{(100)} = 57 \text{ kcal mol}^{-1} \), versus \( E_a \) \( \text{(110)} = 59.5 \text{ kcal mol}^{-1} \) and \( E_a \) \( \text{(111)} = 61 \text{ kcal mol}^{-1} \). Those values are in-between the Si-H bond energy, 47 kcal mol.\(^{-1}\) and the Si-Cl bond energy, 90 kcal mol.\(^{-1}\) (1 eV = 23.053 kcal mol.\(^{-1}\)). Such high activation energies are most probably due to increased surface coverages by Cl atoms (instead of almost exclusively H atoms) for high dichlorosilane mass-flows.
Dangling bond densities on (110) and on (111) surfaces are $1/\sqrt{2}$ and $1/\sqrt{3}$ times that on (100) surfaces, respectively. 29% (42%) lower Si growth rates on (110) (on (111)) than on (100) would then be expected based on such simple considerations (surface reconstructions notwithstanding). Those theoretical values are not far away from those experimentally obtained. Indeed, the Si growth rates on (110) (on (111)) are on average 25% (36%) lower than on (100) in the 700°C–850°C range. Such findings are in line with those reported in [PRI 11] and references therein.

The main features of the 20 Torr growth kinetics of SiGe using a gaseous mixture of dichlorosilane and germane (GeH$_4$) will be described in the coming figures. The SiGe growth rate and Ge concentration functions of the F(GeH$_4$)/F(SiH$_2$Cl$_2$) Mass Flow Ratio (or MFR) are provided in Figure 10.

![Graph showing SiGe growth rate and Ge concentration as functions of F(GeH$_4$)/F(SiH$_2$Cl$_2$) Mass Flow Ratio for different temperatures between 550°C and 750°C.](image)

**Fig. 10.** SiGe growth rate (top) and Ge concentration (bottom) at 20 Torr functions of the F(GeH$_4$)/F(SiH$_2$Cl$_2$) Mass-Flow Ratio for different temperatures between 550°C and 750°C ((100) surface orientation data). The F(SiH$_2$Cl$_2$)/F(H$_2$) MFR, equal to 0.003 for $550°C \leq T \leq 700°C$, was multiplied by 4 at 750°C (i.e. 0.012) to reach low Ge contents. 300 mm data. [HAR 12].
for temperatures between 550°C and 750°C and a (100) surface orientation [HAR 12].

As previously shown, in another 200 mm epitaxial reactor [HAR 07] $x$, the concentration of Ge, increases sub-linearly with the $\text{GeH}_4$ flow. Such behavior is accurately described by a relationship of the type $x^2/(1 - x) = n^* \text{F(\text{GeH}_4)}/\text{F(\text{SiH}_2\text{Cl}_2)}$, with $n = 0.98$ (700°C), 1.34 (650°C), 2.01 (600°C) and 2.52 (550°C).

The exponential increase of $n$ as $T$ (the absolute growth temperature) decreases may be modeled by $n = 5.2 \times 10^{-3} \exp(0.45 \text{ eV}/k_B T)$. The Suh and Lee model, which gives a physical description of the system and includes the $x^2/(1 - x) = n^* \text{F(\text{GeH}_4)}/\text{F(\text{SiH}_2\text{Cl}_2)}$ formula, translates the fact that each surface Cl atom migrates towards a neighboring Ge atom, before being desorbed [SUH 00]. The SiGe growth rate otherwise increases linearly with the mass flow of $\text{GeH}_4$. This is due to the catalyzed desorption of surface H and Cl atoms (freeing dangling bonds for the adsorption of Si and Ge atoms) due to the presence of Ge atoms ($\text{Ge-H}$ and $\text{Ge-Cl}$ bonds, respectively 37 and 51 kcal. mol.$^{-1}$, are weaker than $\text{Si-H}$ and $\text{Si-Cl}$ bonds, 47 and 90 kcal. mol.$^{-1}$). However, the growth rate decreases and the Ge concentration increases when the growth temperature drops, making the 550°C selective epitaxy of SiGe layers rather complicated, at least with a $\text{SiH}_2\text{Cl}_2 + \text{GeH}_4$ mixture (prohibitively low growth rates for Ge contents below 35%).

The complexity of the situation increases when hydrochloric acid is added to the gaseous mixture, which is done, for instance, to promote selectivity versus SiN [HAR 07], [HAR 12]. At 650°C and 20 Torr, a growth rate drop of approximately 50% occurs with $\text{F(\text{HCl})}/\text{F(\text{H}_2)} = 0.0015$ (top part of Figure 11). The SiGe growth rate increase with the germane flow, while being smaller, is also linear. Adding HCl leads to an increase in the concentration of Ge (bottom part of Figure 11).

In the gaseous phase, the added Cl atoms bond preferentially with Si, as the Si chlorides and chlorosilanes are more stable than the corresponding molecules formed with Ge (hence the Ge content increase). The increase of $x$ with the $\text{F(\text{GeH}_4)}/\text{F(\text{SiH}_2\text{Cl}_2)}$ MFR is also sub-linear, with $n = 2.06$. Although the addition of $\text{B}_2\text{H}_6$ leads to a slight increase in the growth rate (no more than 25% here, with a $2 \times 10^{20}$ cm.$^{-3}$ B atomic concentration), it is difficult to selectively deposit SiGe:B RSDs below 650°C (as growth rates are then too low for Ge concentrations below 40%, [HAR 08], [HAR 11b]).

We have quantified in [DES 10] the impact of surface orientation (e.g. (100) and (110)) on the 20 Torr growth kinetics of SiGe at 600°C and 650°C. As expected, the SiGe growth rate decreases as the growth
Fig. 11. SiGe growth rate (top) and Ge concentration (bottom) at 650°C and 20 Torr (versus the $F(\text{GeH}_4)/F(\text{SiH}_2\text{Cl}_2)$ Mass Flow Ratio) without or with HCl ($F(\text{HCl})/F(\text{H}_2) = 0.0015$, then). The $F(\text{SiH}_2\text{Cl}_2)/F(\text{H}_2)$ MFR was equal to 0.003. 300 mm data, (100) surface orientation. [HAR 12].

The discrepancy between the two surface orientations (which will come to the fore when growing SiGe on fins or trigate structures with (110)
sidewalls and (100) tops), is well illustrated by Figure 12 plot of the SiGe growth rate as a function of the Ge content at 600°C and 650°C.

Growing stacks on substrates other than bulk Si can otherwise have a definite impact on growth kinetics. In order to illustrate this, we have deposited at 650°C, 20 Torr a 15 periods \( \{ \text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si} \} \) superlattice on top of a \( \{ 145 \text{ nm thick buried oxide}/15 \text{ nm thick Si over-layer} \} \) SOI(100) substrate. We have plotted in Figure 13 the evolution with the deposited thickness of the Si and SiGe growth rates (top) and the Ge concentration (bottom). We are faced with growth rates which are at first 5% higher than bulk values. They drop down as the deposited thickness increases, reaching a minimum at around 100 nm (70% of the bulk growth rate). Growth rates then go back up. Values close to those on bulk Si(100) are reached for roughly 300 nm of deposited material. Growth rates then decrease once again. The evolution of the Ge concentration with the deposited thickness is the exact opposite of the SiGe growth rate. It reaches a maximum at around 100 nm (21.5%) and goes back to the bulk value (20.2%) for roughly 300 nm. Everything points out towards a surface temperature which is, because of the presence of the buried oxide, lower than the nominal one and which evolves with the deposited thickness. The same trend was evidenced (for the same growth settings) in another 200 mm tool with infra-red pyrometers instead of thermocouples as in Figure 13 [HAR 09]. The evolution of the
Si, SiGe, and Si$_{1-y}$C$_y$ on Si: Epitaxy of Group-IV Semiconductors for Nanoelectronics

Fig. 13. (top) Si and SiGe growth rates together with (bottom) Ge content (bottom) as a function of deposited thickness on 300 mm blanket SOI substrates. Data coming from SIMS depth profiling of the Si and Ge contents in a Si$_{0.8}$Ge$_{0.2}$/Si superlattice grown at 650°C, 20 Torr with SiH$_2$Cl$_2$+GeH$_4$ (SiGe) or SiH$_4$(Si). The starting SOI(100) substrates consisted in 15 nm thick Si layers on top of 145 nm thick buried oxide. J. M. Hartmann et al., unpublished results.

effective surface temperature was then as follows: from 651°C down to 638°C (100 nm), back up to 648°C (350–450 nm) and finally slowly decreasing to 646°C (for 800 nm). Growth kinetics also change with the buried oxide thickness [HAR 03a], [HAR 04b]; this will also have to be factored in when performing epitaxy on SOI wafers.

We are also faced, when working on patterned wafers, with global and local loading effects that are most troublesome in order to obtain SiGe layers of controlled thickness and composition [HAR 04b], [KOL 10], [KOL 11]. By “global” loading effects, we mean the definite growth rate increase and the slight Ge concentration increase that occurs when switching from blanket to patterned wafers. The amplitude of this phenomenon will be inversely proportional to the mask opening, e.g. the amount of the surface that is
not covered by dielectrics. By “local” loading effects, we mean the growth rate and Ge concentration increase that occur when switching from large, closely packed Si windows to small, isolated ones. As an illustration, we have plotted in Figure 14 the normalized growth rates (e.g. the growth rate in a window divided by the growth rate on blanket wafers) at 700°C, 20 Torr for given SiH$_2$Cl$_2$ and GeH$_4$ flows and various HCl flows [HAR 03b]. Without any HCl, we have a factor 4 increase of the growth rate, which is due to a small mask opening: 8% only of the surface (the remainder is covered by SiO$_2$), versus 30%–40% in typical patterns. Adding HCl reduces the growth rate discrepancy, however. We otherwise see that the growth rate fluctuates with the window size.

1.5. Use of low temperature SEG in actual devices

We will describe in the following some successful uses of low temperature H$_2$ bakes and selective epitaxial growth for the fabrication of planar [LER 11] and nanowires-based [BAR 14] pMOSFET transistors with state of the art electrical performances. In order to modulate the threshold voltage $V_T$ and have a high mobility channel for holes in [LER 11] devices, a $\{\text{Si}_{0.8}\text{Ge}_{0.2}\text{3 nm}/\text{Si 2 nm}\}$ bilayer was grown at 650°C and 20 Torr with SiH$_2$Cl$_2$+GeH$_4$ (using Figure 10 data points) on a 300 mm Extra-thin (ET-)SOI substrate (starting Si thickness around 3 nm). A “HF-Last” wet
cleaning followed by an in-situ H\textsubscript{2} bake at 650°C and 20 Torr for two minutes (in order to avoid any islanding of the very thin Si starting layer) was used to prepare the surface beforehand. A second epitaxy was then carried out later on in the process flow (after gate stack deposition and patterning) in order to selectively grow highly in-situ B doped Si\textsubscript{0.7}Ge\textsubscript{0.3} raised sources and drains ([B] = 2 × 10\textsuperscript{20} cm\textsuperscript{-3}). This drastically reduces the access resistance of the transistors and to a certain extent, introduces a uniaxial compression in the SiGe channel, increasing the hole mobility. As with the channel, a temperature of 650°C was used for both the in-situ H\textsubscript{2} bake and the SiGe:B epitaxy (with a SiH\textsubscript{2}Cl\textsubscript{2} + GeH\textsubscript{4} + HCl + B\textsubscript{2}H\textsubscript{6} chemistry; cf. [HAR 13a]). Cross-sectional Transmission Electron Microscopy images of a pMOSFET transistor (gate length: 30 nm) and of the channel beneath its gate are shown in Figure 15. The \{Si\textsubscript{0.8}Ge\textsubscript{0.2}/Si\} bilayer has a perfect crystallinity (no extended defects; abrupt interfaces). The deposition process used for the Si\textsubscript{0.7}Ge\textsubscript{0.3}:B raised sources and drains is otherwise perfectly selective versus the Si\textsubscript{3}N\textsubscript{4} spacers. \{111\} facets are however present at the boundaries between the source and drain regions and the gate.

Short gate length epitaxial SiGe/Si multi-(core/shell) p-type nanowire (NW) transistors were fabricated in [BAR 14]; a cross-sectional TEM picture

![Fig. 15. Cross-sectional High Resolution TEM images of a pMOSFET transistor (of 30 nm gate length) with a SiGe/Si bilayer as channel for the holes and silicided, 18 nm thick Si\textsubscript{0.7}Ge\textsubscript{0.3}:B raised sources and drains. 300 mm data, (100) surface orientation for the starting ET-SOI substrate. [LER 11].](image-url)
Fig. 16. (a) Cross sectional TEM image of a SiGe/Si multi-(Core/Shell) P-FET nanowire transistor with a 15 nm gate length (Inset: Energy Dispersive X-ray analysis of a core-shell NW with a HfSiON/TiN metal gate). (b) Cross-section of a hexagonal multi-(Core/Shell) nanowire with \{(111)\} facets. (c) Effective hole mobility in nanowire (full lines) and planar (dotted lines) MOSFETs, the channel being either Si or SiGe/Si Strained Layer Superlattices (SLS). Mobility is higher in the latter than in the former, all the more so in NW devices. 300 mm data. [BAR 14].

of such a device can be found in Figure 16(a). To that end, silicon nanowires with \{(110)\} sidewalls and \{(100)\} top surfaces were first of all patterned in \{(100)\} ET-SOI wafers by lithography and etching [BAR 12]. A “HF-Last” wet cleaning followed by a 2 min. H₂ bake at 650°C, 20 Torr was then used to remove native oxide and have Si NW surfaces fit for growth.
Dichlorosilane and germane were subsequently used for the 650°C, 20 Torr SEG of Si_{0.7}Ge_{0.3}/Si/Si_{0.7}Ge_{0.3}/Si shells around the Si NW cores (using once again Figure 10 data points). The formation of epitaxial SiGe facets along the \{111\} crystallographic planes is obvious in Figure 16(b). The access regions on each side of the \{HfSiON/TiN/poly-Si\} gates were later on thickened thanks to a 650°C, 20 Torr SEG of 18 nm thick Si_{0.7}Ge_{0.3}:B layers. Electrical transport measurements showed a hole mobility improvement up to 100% in SiGe/Si multi-(core/shell) NWs (70% in wide planar devices) compared to p-type Si p-MOSFETs; see Figure 16(c). A drive current enhancement of 60% compared to reference Si-channel devices was otherwise evidenced in multi-(core/shell) P-FET NWs scaled down to 15 nm gate length. The [BAR 14] paper on those results won the 2014 IEEE EDS Paul Rappaport Award.

1.6. Advanced low temperature cyclic deposition/etch processes for recessed and raised sources and drains

We have recently shown that silane (SiH₄) and disilane (Si₂H₆) yielded vastly higher growth rates at low temperatures than dichlorosilane (SiH₂Cl₂) [HAR 12], [HAR 14a]. Such gases are intrinsically not selective versus dielectrics masks, however. This difficulty can be overcome with the so-called Cyclic Deposition/Etch (CDE) process, which was patented in 2006 by Bauer et al. [BAU 06], [BAU 07]. The general principle of this technique is as follows: a few nm of the desired material is deposited not selectively on patterned wafers, usually with high order silanes such as disilane (Si₂H₆) [LOU 12] or trisilane (Si₃H₈) [BAU 12a] (which delivers high growth rates at low temperatures [GOU 09], [TAK 10], [VIN 10]). Single-crystalline layers are then grown in the Si active area of those wafers, whereas poly-crystalline or amorphous layers are deposited on top of dielectrics. A selective etch of the latter type of layers is then performed using Cl₂ [BAU 12a], HCl + GeH₄ [BAU 12b] and so on. A thin single-crystalline layer is then obtained in the active area of patterned wafers, while dielectrics layers are free of deposits. The repetition of growth and etch steps (hence the “Cyclic Deposition/Etch” name) yields the active layer thickness aimed for, with full selectivity (see Figure 17 schematics inspired from [VER 07]).

CDE is usually conducted at low temperatures (≤600°C) for several practical reasons: (i) as far as Si_{1−y}Cₙ:P layers are concerned, the lower the temperature and the higher the growth rate are, the higher the substitutional C content in those layers will be [HAR 4c], [BAU 07]; (ii) high Ge content
SiGe:B layers as in [HE 12] will remain fully compressively strained and (iii) amorphous layers deposited at low temperatures on dielectrics will be etched much faster (compared to single-crystalline layers) than higher temperature poly-crystalline layers [HAR 10], [BAU 12b].

Trisilane, one of the Si precursors of choice for CDE, has several drawbacks: (i) it is extremely expensive to produce with electronic-grade quality; (ii) being liquid, it requires a dedicated bubbler to be delivered into the growth chamber. Cl₂, the CDE etching gas advocated by Bauer et al., needs to be injected in the growth chamber in dedicated supply lines, in order to avoid exothermic reactions with trisilane [BAU 12a]. A Si₂H₆ + SiCH₆ + PH₃ chemistry has recently been used by Loubet et al. to fabricate Si₁₋ᵢCᵢ₋ᵢP RSDs with a CDE approach (using HCl as the etchant gas) [LOU 12]. There is however a scarcity of results in the literature concerning the use of disilane for the low temperature growth of group IV layers. We have therefore benchmarked SiH₄ and Si₂H₆ for the (001) growth of Si:P and Si₁₋ᵢCᵢ₋ᵢP. We have also quantified the beneficial impact of adding GeH₄ to HCl in order to etch Si at low temperatures [HAR 13b]. Knowing the specifics of individual growth and etch steps (i.e. steps (a) and (b) of Figure 17) has enabled us to develop new 300 mm Si, Si:P and Si₁₋ᵢCᵢ₋ᵢ:P CDE processes [HAR 13c], whose main features are summed up in the following.

Major differences between silane and disilane concerning the low temperature in-situ phosphorous doping of Si(100) have been identified, as shown in Figure 18. Phosphorous surface segregation has prevented us
from reaching $P^+$ ion concentrations higher than a few $10^{19}$ cm$^{-3}$ with SiH$_4$; the resulting surface “poisoning” led to a severe growth rate reduction (at 650°C, 20 Torr). Meanwhile, $[P^+]$ increased linearly with the phosphine flow when using Si$_2$H$_6$ as the Si precursor; values as high as $1.7 \times 10^{20}$ cm$^{-3}$ were achieved. The Si:P growth rate from Si$_2$H$_6$ was initially stable then increased as the PH$_3$ flow increased (at 550°C, 20 Torr).

Similar substitutional C concentrations $[C]_{\text{subst.}}$ were achieved in intrinsic Si$_{1-y}$C$_y$ layers grown at 550°C, 20 Torr with both Si gaseous precursors (up to 1.9%), although growth rates were approximately 6 times higher with Si$_2$H$_6$ than with SiH$_4$. (e.g. 3 instead of 0.5 nm min.$^{-1}$). Mono-methylsilane
Flows 6.5 to 10 times higher were needed with \( \text{Si}_2\text{H}_6 \) than with \( \text{SiH}_4 \) to obtain the same \([C]_{\text{subst.}}\) on (100), as illustrated in Figure 19. Finally, \( \sim 30 \text{ nm} \) thick \( \text{Si}_{1-y}\text{C}_y \) layers became rough as the substitutional C content exceeded 1.6\% (formation of numerous small size islands, as in [HAR 10], [SHI 12]).

We have then studied the structural and electrical properties of “low” and “high” C content \( \text{Si}_{1-y}\text{C}_y\):P layers (~1.5 and 1.8\%, respectively) grown at 550°C, 20 Torr with \( \text{Si}_2\text{H}_6 \). Adding significant amounts of \( \text{PH}_3 \) led to a reduction of the tensile strain in the films (still high crystalline quality in X-ray Diffraction). This was due to the incorporation of P atoms (at the expense of C atoms) in the substitutional sites of the Si matrix. \( \text{Si}_{1-y}\text{C}_y\):P layers became rough as the \( \text{PH}_3 \) flow increased. Resistivities lower than 1 mOhm.cm were nevertheless associated with those \( \text{Si}_{1-y}\text{C}_y\):P layers, with P atomic concentrations up to \( 4 \times 10^{20} \text{ cm}^{-3} \).

We have otherwise quantified the etch rate increase occurring when adding comparatively small amounts of \( \text{GeH}_4 \) to HCl (etching of single-crystalline Si). Etch rates were almost the same for temperatures 1000°C and above. There was however a growing discrepancy at lower temperatures, with 12–36 times higher Si etch rates achieved at 20 Torr with HCl + \( \text{GeH}_4 \) than with pure HCl (the first atomic mono-layers became “SiGe-like” and
were etched must faster. Workable etch rates (i.e. close to 1 nm min$^{-1}$) were obtained at 600°C (versus 750°C for pure HCl), as shown in Figure 20. A chamber pressure increase otherwise helped us in reaching higher etch rates.

We have then evaluated various CDE processes in order to selectively grow at low temperatures Si, Si:P and Si$_{1-y}$C$_y$:P Raised Sources and Drains on patterned SOI(100) wafers. A Si$_2$H$_6$+Ph$_3$+SiCH$_6$ chemistry was used for the 550°C growth steps. Meanwhile, the selective etch of layers on dielectrics was conducted at 600°C with HCl + GeH$_4$.

We have first of all studied the specifics of those isobaric (P = 20 Torr) CDE processes on bulk, blanket Si(001) substrates. High crystalline quality
and smooth CDE-grown Si, Si:P and Si$_{1-y}$C$_y$(P) layers were produced. However, 2–3% Ge was injected in the layers during the etch steps. These Ge atoms, being larger than Si and C atoms, reduced the tensile strain and thus the “apparent” substitutional C content [C]$_{\text{subst.}}$ in the Si$_{1-y}$C$_y$(P) layers (from X-ray Diffraction). This [C]$_{\text{subst.}}$ reduction, close to 0.2%, occurred as soon as etch steps were used, with little or no dependence on the etch time per step. The two SiCH$_6$ mass-flows probed yielded [C]$_{\text{subst.}}$ = 1.3% and 1.6% in our CDE-grown Si$_{1-y}$C$_y$ layers. Although process conditions were the same, [C]$_{\text{subst.}}$ was slightly lower in Si$_{1-y}$C$_y$:P layers (~0.1%). This was likely due to the incorporation of large amounts of P atoms at the expense of C atoms in the lattice. The atomic P concentration in our Si:P and Si$_{1-y}$C$_y$:P layers was indeed higher than $2 \times 10^{20}$ cm$^{-3}$. The Si, Si:P and Si$_{1-y}$C$_y$(P) thickness deposited per CDE cycle decreased linearly as the HCl+GeH$_4$ etch time increased. The “equivalent” etch rate (e.g. the slope of this linear decrease) was lower in intrinsic than in in-situ doped layers, however. The higher the C content was, the lower the etch rate otherwise was (0.53 nm min.$^{-1}$ for Si:P, versus 0.23 nm min.$^{-1}$ for “high” C content intrinsic Si$_{1-y}$C$_y$). A CDE strategy suppressed the islanding occurring for high C content, several tens of nm thick Si$_{1-y}$C$_y$:P layers grown in one step only (as in [SHI 12]). The resistivity of our Si$_{1-y}$C$_y$:P layers did not depend on the growth mode. It however increased with the C content, as in [LOU 12], from 0.48 mOhm.cm ([C]$_{\text{subst.}} = 0\%$) up to 0.87 and finally 1.06 mOhm.cm ([C]$_{\text{subst.}} = 1.3\%$ and 1.6\%).

We have then calibrated, for 19–23 nm thick CDE-grown Si, Si:P and Si$_{1-y}$C$_y$:P RSDs, the HCl + GeH$_4$ etch time/step necessary to achieve full selectivity on patterned SOI(100) substrates. Selectivity was obtained for intrinsic Si as soon as 180s etch steps were used. Longer etch times were needed for Si:P and especially Si$_{1-y}$C$_y$:P (270 and 315s/CDE cycle, respectively).

The resulting S/D areas were rather smooth and slightly faceted, but as the poly-Si layers sitting on top of the gate stacks were unprotected with the integration scheme used here, they were completely removed with such etch times, as shown in Figure 21. Hard masks will thus have to be used in actual devices. Finally, we have compared the Si, Si:P and Si$_{1-y}$C$_y$:P layer thickness deposited per cycle on bulk, blanket Si and in the large metrology windows of patterned ET-SOI substrates. Similar values were obtained in all cases. Global loading effects are thus negligible.
Fig. 21. Top view and cross-sectional SEM images of 300 mm ET-SOI transistors after the CDE of 21–22 nm thick Si:P layers in the source/drain regions. Growth steps: $T = 550\,^\circ\text{C}, P = 20$ Torr, $F(\text{Si}_2\text{H}_6)/F(\text{H}_2) = 0.003 + F(\text{PH}_3)/F(\text{H}_2) = 6 \times 10^{-5}$, growth time = 30s/CDE cycle. Etch steps: $T = 600\,^\circ\text{C}, P = 20$ Torr, $F(\text{HCl})/F(\text{H}_2) = 0.167 + F(\text{GeH}_4)/F(\text{H}_2) = 1.33 \times 10^{-3}$, etch time = 180s or 270s/CDE cycle. Number of CDE cycles increased from 7 to 9 in order to have similar thicknesses. [HAR 13c].

We have otherwise leveraged our know-how on (i) disilane-based epitaxial growth and (ii) Cyclic Deposition/Etch strategies to develop an innovative 500$^\circ$C process for the 300 mm selective deposition of heavily in-situ boron-doped SiGe:B RSDs on (100) ET-SOI wafers [HAR 14b] [Lu 16]. We have first of all evaluated the impact of diborane on the 500$^\circ$C, 20 Torr growth kinetics of SiGe:B on blanket Si(001).

The growth rate significantly increased while the Ge content decreased as $\text{B}_2\text{H}_6$ was added to disilane + germane: from 3 up to 13 nm min.$^{-1}$ and from 45% down to 28%, respectively (see Figure 22). Layers were of excellent crystalline quality even for high substitutional B concentrations (from strain compensation: at most $5 \times 10^{20}$ cm$^{-3}$). The lowest resistivity achieved, $\sim 4 \times 10^{-4}$ Ohm.cm, was a factor of two lower than our usual 650$^\circ$C process (see Figure 23). Electrically active boron concentrations were otherwise as high as $7.5 \times 10^{20}$ cm$^{-3}$.
We have then studied whether or not straightforward SiGe:B SEG was feasible by adding HCl, an etchant gas that promotes selectivity on patterned wafers, to the gaseous mixture. As expected, the (100) SiGe:B growth rate decreased while the Ge content increased with the HCl flow. The poly-SiGe:B growth rate on SiO2-covered Si wafers was close to the single-crystalline growth rate on blanket Si wafers, however (even for high HCl flows): see Figure 24. Co-flow SEG is thus not feasible at 500°C with Si₂H₆+GeH₄+HCl.

Fig. 22. SiGe:B growth rates (top) and real or “apparent” Ge concentrations (bottom) associated with SiGe:B layers grown at 500°C, 20 Torr with Si₂H₆+GeH₄+HCl and various amounts of B₂H₆. Strain compensation by B atoms, which are much smaller than Si and Ge atoms, explains why “Apparent Ge” contents from XRD are smaller than “Real” Ge contents from X-ray Fluorescence. [HAR 14b].
Fig. 23. Resistivity associated with the SiGe:B layers grown at 500°C, 20 Torr with Si$_2$H$_6$+GeH$_4$+HCl and various amounts of B$_2$H$_6$. Same layers as in Figure 22. 300 mm data, (100) surface orientation. [HAR 14b].

Fig. 24. Single crystalline and poly-crystalline SiGe(:B) growth rates at 500°C, 20 Torr for various F(HCl)/F(H$_2$) mass-flow ratios. The F(Si$_2$H$_6$)/F(H$_2$), F(GeH$_4$)/F(H$_2$) and F(B$_2$H$_6$)/F(H$_2$) MFRs were constant and equal to 0.0015, 0.0014 and $6.67 \times 10^{-6}$, respectively. 300 mm data. [HAR 14b].
We have then benchmarked various CDE strategies in order to obtain the selectivity aimed for at 500°C. The overall deposition time was constant at 432s, while various HCl partial pressures and total etch pressures were tested in simple Deposition/Etch (DE) processes or 12 cycles CDE processes. For cyclic processes, low HCl flows and etch pressures (20 Torr) resulted in almost nil poly-SiGeB etch rates (0.4 nm min.\(^{-1}\) only). Significantly increasing both the HCl flow and the total etch pressure (80 Torr) delivered the poly-SiGe:B etch rates sought after (4 nm min.\(^{-1}\)). The etch selectivity (i.e. the poly-SiGe:B etch rate on SiO\(_2\)-covered substrates divided by the SiGe:B etch rate on blanket Si) was low, however (2.7 only). The resulting SiGe:B layers were otherwise 3D for long etch durations, making such CDE processes worthless (as for chlorinated chemistries at 650°C [HAR 13a]).

We have thus used a simpler 500°C DE process, with a single etch step at 740 Torr (atmospheric pressure) after the 20 Torr growth of the whole layer. Etch selectivity was improved when switching from high to medium HCl flows (from 2.6 up to 4.8), while still having high poly-SiGeB etch rates (24 nm min.\(^{-1}\)):

![Fig. 25.](image)

**Fig. 25.** Single crystalline and poly-crystalline SiGe:B layer thickness as a function of the HCl etch time for the optimum 500°C DE process. Si\(_{0.65}\)Ge\(_{0.35}\):B deposition at 20 Torr lasted 432s with constant Si\(_2\)H\(_6\), GeH\(_4\) and B\(_2\)H\(_6\) mass-flows. Meanwhile, the HCl etch step was conducted at \(P = 740\) Torr with a low \(F(\text{HCl})/F(\text{H}_2)\) mass-flow ratio (0.2). 300 mm data.
gate stacks and studied the feasibility of such a DE process. Longer HCl etch times than the ones identified on blanket wafers were key in getting rid of poly-SiGe:B on top of dielectrics covered surfaces such as the SiO$_2$ isolation or the SiN spacers; rather smooth, facetted SiGe:B raised sources and drains were obtained in the end: see Figure 26.

Fig. 26. 3 dimensional or top view SEM images of single and multi-fingered FETs on patterned ET-SOI or Ge-enriched ET-SiGeOI wafers ([GLO 14]) with gate stacks after the 500°C Deposition/Etch of SiGe:B RSD. Si$_{0.65}$Ge$_{0.35}$:B deposition occurred at 20 Torr with constant $F$(Si$_2$H$_6$)/$F$(H$_2$), $F$(GeH$_4$)/$F$(H$_2$), $F$(HCl)/$F$(H$_2$) and $F$(B$_2$H$_6$)/$F$(H$_2$) mass-flow ratios ($0.0015$, $0.0014$, $0.001$ and $1.67 \times 10^{-6}$, respectively). Meanwhile, the HCl etch steps were conducted at $P = 740$ Torr with a low $F$(HCl)/$F$(H$_2$) MFR ($0.2$). 300 mm data, (100) surfaces. [HAR 14b].
1.7. Conclusions and some short term perspectives

In this chapter, we have presented some of the challenges one faces when selectively growing group-IV semiconductors on patterned wafers for nanoelectronics, namely: surface preparation, faceting, loading effects, surface temperature changes because of the presence of a buried oxide and so on. We have described some of the salient features of the chlorinated chemistry used for Selective Epitaxial Growth (e.g. SiH₂Cl₂ + GeH₄ + HCl) and shown two successful uses of that chemistry in advanced planar or core-shell based Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Finally, we have detailed a new type of process that yields low temperature selectivity, e.g. the Cyclic Deposition/Etch (CDE) approach. It consists in growing Si (Si:P, SiC:P) or SiGe:B non selectively on patterned wafers, then selectively removing poly-crystalline materials (on dielectrics) while keeping some single-crystalline layers inside Si (or SiGe) windows.

Let us now discuss some current and near future group-IV epitaxy trends. Very low temperature (e.g. T \leq 500^\circ C) epitaxy (with the use of CDE) has some major appeal, as it would enable monolithic 3D integration, e.g. the sequential processing of layers of ET-SOI transistors one upon the other (with metallic interconnections in-between) [FEN 14], [BAT 15], avoid 3D objects’ (such as fins or tri-gates) shape changes and so on. Liquid Si precursors such as trisilane (Si₃H₈), tetrasilane (Si₄H₁₀, [KAN 93], [HAZ 16], [HART 16]) neopentasilane (Si₅H₁₂, [CHU 08]) and so on together with slightly more evolved Ge precursors such as digermane (Ge₂H₆, [WIR 13], [HAR 16]) will then be most handy (in combination with Cl₂ as the low temperature etchant gas).

The Ge content in the embedded or raised SiGe:B Sources and Drains (S/Ds) on each side of high performance p-type MOSFETs becomes higher and higher when moving from one technology node to the next one (50% for the 22 nm technology node [HYK 14]), in order to inject higher and higher amounts of uniaxial compressive strain in the channel of planar [DEN 12] and now fin-shaped devices. The low temperature selective epitaxy of Ge-rich SiGe layers (e.g. with Ge contents above 50%) will thus continue to be explored.

Such know-how will also be beneficial for the high Ge content SiGe cladding of Si FinFETs, with therefore some superior hole mobilities [MER 14]. Several hundreds of nm thick Ge layers selectively grown in deep, narrow cavities (with a Si floor and SiO₂ sidewalls) can benefit from Aspect Ratio Trapping, resulting in rather low defect density, relaxed layers that can be used as the core of high mobility Ge FinFETs [VAN 14] (presence
of Ge(110) planes, then). A variant of this approach is to selectively grow Ge$_x$Si$_{1-x}$ buffers (with $x$ typically in the 70%–85% range) instead of pure Ge in those cavities, followed by the epitaxy of thin, compressively-strained Ge layers, with therefore better transport properties than in unstrained Ge [MIT 14].

Fig. 27. (top) cross-sectional Transmission Electron Microscopy images of a Si multi-channel FET with SiN internal spacers and Si raised Sources and Drains [HAR 10]. The SiGe1, 2 and 3 layers still present in the left picture were selectively etched and the voids filled with \{HfO$_2$/TiN/N$^+$ poly-Si\} gate stacks (G1, G2 and G3 in the right picture). (bottom) Introduction of SiN internal spacers adds only four steps to the MCFET process flow sequence. 200 mm data. [BER 09].
One could otherwise use SiP binary alloys (instead of “regular” SiC:P films) in the S/D regions of n-MOSFETs. Although P atoms are not as small as C atoms (aP = 5.014 Å instead of aC = 3.567 Å and aSi = 5.431 Å), the uniaxial tensile strain in short gate length devices will indeed be high if the P concentration is high (at most: 12% in [WEE 12]). This will most likely boost the mobility of electrons in short gate length n-MOSFETs.

Finally, using SiGe/Si multilayers together with sacrificial etching enables to fabricate stacked NWs with superior integration densities and device performances ([BER 09], [TAC 09], [BAR 15]), as shown in Figure 27. Fins with Ge fluctuations along the z axis are defined during the process (prior to the lateral selective etching of SiGe or Si). Ge enrichment (e.g. the high temperature thermal oxidation of SiGe, with a preferential oxidation of Si atoms and a “snowplough” effect for the Ge atoms) might also be handy during device fabrication [GLO 14], [NGU 14]. Such stacked NWs might therefore be the ultimate evolution (and the convergence point) of the finFET and the FD-SOI technologies.

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