Effect of size and position of gold nanocrystals embedded in gate oxide of SiO₂/Si MOS structures

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Received 5 November 2015; Revised 29 November 2015; Accepted 1 December 2015; Published 5 February 2016

The influence of single and double layered gold (Au) nanocrystals (NC), embedded in SiO₂ matrix, on the electrical characteristics of metal–oxide–semiconductor (MOS) structures is reported in this communication. The size and position of the NCs are varied and study is made using Sentaurus TCAD simulation tools. In a single NC-layered MOS structure, the role of NCs is more prominent when they are placed closer to SiO₂/Si–substrate interface than to SiO₂/Al–gate interface. In MOS structures with larger NC dots and double layered NCs, the charge storage capacity is increased due to charging of the dielectric in the presence of NCs. Higher breakdown voltage and smaller leakage current are also obtained in the case of dual NC-layered MOS device. A new phenomenon of smearing out of the capacitance–voltage curve is observed in the presence of dual NC layer indicating generation of interface traps. An internal electric field developed between these two charged NC layers is expected to generate such interface traps at the SiO₂/Si interface.

Keywords: Nanocrystals; MOS; capacitance–voltage curve; leakage current.

1. Introduction

In recent days, nonvolatile memory (NVM) devices utilizing discrete nanocrystals (NC) as floating gate have received considerable attention due to their excellent memory applications. Among NC memories, metal NCs have a number of advantages over their semiconductor counterpart, including higher density of states around the Fermi level, stronger coupling with the conduction channel, a wide range of available work functions, and smaller energy perturbation due to carrier confinement.¹ Among the various species of metallic nanoparticles, gold (Au) has been reported to be chemically stable, be easily synthesized, and of high work function.² High work function of Au provides a high confinement barrier in the retention mode and a relatively low barrier in the programming and erasing modes. NCs are embedded between the layers of control oxide and tunneling oxide of a metal–oxide–semiconductor (MOS) structure. The NCs, typically organized in a two-dimensional array in between dielectrics, act as discrete charge storage nodes and the trapped charge is retained for a longer time than in conventional floating gate flash memories due to quantum effects. As a result, the devices can be less sensitive to local oxide defects.

In order to study the role of NCs in determining the electrical properties of a MOS capacitor, we investigate the performance of the capacitor for NVM application using Sentaurus TCAD tools.³ Au NCs are embedded within the gate oxide. The electrical characteristics of MOS capacitor

are simulated by changing position of the NC layer, and finally introducing a dual layer of Au NCs embedded in SiO₂ matrix. In all cases, size of the NC is also varied and the corresponding results are discussed.

2. Simulation Work

Since MOS capacitor type flash memory devices can be simply fabricated without source/drain junctions, the prototypes of NC-based memory devices have been simulated using Sentaurus TCAD with a MOS capacitor structure. The typical structure of a dual NC layered MOS capacitor memory device is shown in Fig. 1. The memory device is simulated on *p*-type Si substrate with a thin tunneling oxide layer of SiO₂. Two layers of Au NCs are embedded in the tunneling oxide layer. The controlling oxide, SiO₂ is then deposited and finally, the gate electrode (Al) is formed and patterned to yield MOS capacitor structure for memory devices.

Thickness of the SiO₂ gate oxide layer is taken here as 15 nm, within which spherical Au NCs are embedded at regular intervals. We start with a single layer of Au NC embedded in SiO₂ matrix very close to the Si substrate (On Si configuration). Next we relocate the layer closer to the Al gate (On Al configuration), and finally the dual layer structure of the NCs as shown in Fig. 1 is obtained where the NC layers are placed symmetrically within the SiO₂. For each of the above configurations, dimension of the dots is changed. For ‘On Si’ structure we consider 0.1-nm thick tunneling

Fig. 1. A typical structure of dual NC layered MOS capacitor.

oxide layer, while for ‘On Al’ structure the control oxide layer is 0.1-nm thick. For ‘Near Si’ and ‘Near Al’ devices, we consider 4-nm thick tunneling and control oxide layer, respectively. Combining both the ‘Near Si’ and ‘Near Al’ layered structures with NC of radius 1 nm, the dual layered NC-based MOS structure is realized (in Table 1).

A high frequency (HF) capacitance–voltage (C – V) curve is simulated at a frequency of 1 MHz at room temperature. The C – V characteristics of the above structures are compared with that of the MOS structure without NCs. The dc gate bias is varied so that all the accumulation, depletion and inversion modes are attained. The leakage current–voltage (I – V) characteristics are also simulated for the MOS structures.

3. Results and Discussions

The C – V curve for the MOS capacitor without any NC shows typical accumulation–depletion–inversion characteristic with a flat band voltage (V_{fb}) of -0.5 V and is presented in Figs. 2 and 3 as a reference one. The negative value of the flat band

voltage can be attributed to the presence of cationic ions viz. Na^+ ions within the control oxide layer or the positively charged interfacial states at the SiO_2/Si interface in the MOS structure.⁴

The C – V characteristics of the ‘On Si’ and ‘On Al’ configurations are demonstrated in Figs. 2(a) and 2(b), respectively. The C – V curves in Fig. 2(a) for the capacitor with gold nanoparticles demonstrate a significant flat band voltage shift that increases with increase in the dot size. Such shift originates mainly from the presence of Au NCs rather than cationic ions within the control oxide and positive charges at the interface. Since the flat band voltage shift for ‘No dot’ structure is negligible, it can be inferred that injected charges are stored mainly in NC or at their interfaces. In Fig. 2(b), it is further observed that the accumulation capacitance is higher for larger dots. The effective oxide thickness decreases with increase in dot size. Again, with increase of the NC dimension, surface area and thereby, charge storing capacity of the NCs increases. All these facts lead to rise in accumulation capacitance.

The tunnel oxide is thinner for the ‘On Si’ structure compared to a similar ‘On Al’ structure. For a particular size of the NC, the C – V characteristics is more flat for ‘On Si’ structure. Thus, this structure yields higher flat band voltage and maintains good retention characteristics.

The C – V characteristics of MOS structures having a layer of Au NC of radius 1 nm are shown in Fig. 2(c) for different positions of the layer within it. Our simulation begins with the ‘On Si’ configuration, with gradual increase in its tunneling oxide layer thickness i.e., shifting the dots gradually towards the gate metal, and finally reaching the ‘On Al’ position. It appears from the C – V characteristics that the curve possesses steeper transition with increase in tunneling oxide thickness, implying that it approaches gradually the nature for ‘No dot’ configuration. The simulation is repeated with dot of radius 2 nm [Fig. 2(d)]. Comparison of these two set of curves presented in Figs. 2(c) and 2(d) reveals that they are of similar nature, and for larger dot smearing of the curve is much more pronounced.

The C – V characteristics of MOS structures with single NC layer at two positions (Near Si and Near Al) and dual NC layer are shown in Fig. 3. The most sharp transition from accumulation to depletion in the C – V characteristic is observed for the MOS structure without NC. The presence of NC layer either at the semiconductor end or at the metal gate

Table 1. Description of the structures.

Device name	Device description
On Si	Tunneling oxide thickness — 0.1 nm; Control oxide thickness — 14.9 nm
Near Si	Tunneling oxide thickness — 4.0 nm; Control oxide thickness — 11.0 nm
Near Al	Tunneling oxide thickness — 11.0 nm; Control oxide thickness — 4.0 nm
On Al	Tunneling oxide thickness — 14.9 nm; Control oxide thickness — 0.1 nm
Dual layered	Tunneling oxide thickness — 4.0 nm; Control oxide thickness — 4.0 nm

Fig. 2. C - V characteristics of the MOS devices: (a) 'On Si' for different dot dimensions; (b) 'On Al' for different dot dimensions; (c) NC layer with dot radius of 1 nm for different dot positions; (d) NC layer with dot of radius 2 nm for different dot positions.

Fig. 3. C - V characteristics of MOS structures with NCs in single layer at 'Near Si' and 'Near Al' position, and in dual layers.

end increases the accumulation capacitance with a shift in the flat band voltage, indicating storage of charge in the NCs. In the presence of dual NC layer, the C - V curve is smeared out along with a significant shift in V_{fb} due to electron charging. The difference in nature of C - V characteristics may be due to the presence of excessive immobile positive charges in the

oxide layer and the work function difference between Al and Si.⁵ In a recent work, Liu *et al.* proposed that the NCs play a dominant role in the charging effect over the NC/SiO₂ interface.⁶ The dominant mechanism is thus charging of the MOS dielectric in the presence of large number of electrons in Au NCs, and therefore, effect of the traps and defects can be ignored in most of such cases.⁷ Interestingly, a new phenomenon of smearing out of the C - V curve is observed in the case of dual NC layer indicating generation of interface traps. When the MOS structure is biased for accumulation, the NCs in the layer near the gate are positively charged whereas those near the Si substrate are negatively charged. As a result, an electric field is developed between these two charged NC layers. This electric field may give rise to interface traps at the SiO₂/Si interface.

Figure 4 depicts the field distribution within the dielectric in the presence of NCs at different positions. It is observed that in the presence of NCs in the dielectric film, the electric field between the Al electrode and top of the NCs is maximum. The electric field is minimum at the bottom of each NC. A Gaussian profile of electric field is observed at the bottom side of two NCs which is clearly visible for MOS device with NCs near Al. The field shows a maximum in

Fig. 4. Field distribution within the dielectric of different MOS devices.

between two NCs. It is apparent that the electric field generated due to gate voltages is screened by the NCs. A similar phenomenon is observed for the devices with NCs near Si. In case of dual layered NCs, a zero field region is observed in between two NCs aligned in the vertical direction.

Fig. 5. I - V characteristics of 'Near Si', 'Near Al' and 'dual layer' MOS structures.

Figure 5 presents the leakage current characteristics of the above three structures. The significant decrease in leakage current for the dual NC-based MOS device is observed. As carriers are injected into the NC, the Coulomb blockade effect prevents further injection and provides storage of more carriers.⁸ Charges stored in the NC layers develop an internal electric field that partly compensates the external electric field, and makes the leakage current small which is also evident from the electric field distribution in the dielectric in the presence of the NCs as shown in Fig. 4. As a result, a MOS structure with dual NC layers may possess a small leakage current and a much higher breakdown voltage.

4. Conclusion

MOS capacitors with Au NC, selectively embedded in their dielectric layers, are simulated and characterized revealing that the presence of NCs influences the MOS characteristics in various way. A smearing of C - V curve appears in NC layered MOS structure with larger dots. The presence of Au NCs also suppresses leakage through the gate oxide, making

dual NC layered MOS structures suitable for high field applications.

Acknowledgments

The authors wish to acknowledge the University Grants Commission, Government of India for financial assistance. The simulation work is supported by the UGC, UP-II project entitled “Modelling optoelectronic and transport characteristics of semiconductor nanostructures.”

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