Role of interfacial layer thickness on high- κ dielectric-based MOS devices

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An attempt has been made to investigate the role of interfacial layer (IL) and its thickness on HfO_2 -based high- κ metal-oxide-semiconductor (MOS) devices. The capacitance–voltage (C – V) and current–voltage (I – V) characteristics have been simulated using Sentaurus TCAD software for two different IL thicknesses and at different substrate temperatures and doping concentrations. The device performance is found to be improved for an IL thickness of 1 nm at higher temperature but deteriorates with further increase in IL thickness. The capacitance value decreases with the increase in IL thickness and a flatband voltage shift (V_{fb}) due to the presence of interfacial charges at IL of higher thickness is observed. The analysis of I – V curve further shows that the leakage current change is more prominent at lower temperature for different IL thickness. The temperature dependence C – V curves show that the presence of 1 nm IL makes the device more reliable at elevated temperature.

Keywords: MOS; HfO_2/Si interface; high substrate temperature; C – V ; I – V .

1. Introduction

Unavoidable growth of interfacial layer (IL) affecting the performance of the high- κ dielectric-based metal-oxide-semiconductor (MOS) device has now become a problem in achieving its higher dielectric value and lower leakage current. The interfacial SiO_2 is grown either at the time of deposition/growth, a technique-dependent phenomenon, or during annealing. Among the high- κ materials, HfO_2 is considered to be one of the most promising materials^{1–5} that satisfies the requisite properties e.g., higher dielectric constant, better thermal stability with Si ^{6,7} and relatively large bandgap. But, the HfO_2 -based MOS devices also suffer from the problem of interfacial growth of SiO_2 resulting in lower dielectric constant. As a consequence, the development of experimental and simulation methods to address these effects is now of primary importance for achieving HfO_2 -based MOS devices with better electrical properties. The present paper focusses on simulation study of electrical properties of HfO_2 -based MOS devices having different IL thicknesses. The electrical performance of the MOS device is analyzed by extracting the data from the capacitance–voltage (C – V) and current–voltage (I – V) characteristics simulated at room and elevated temperatures. The Sentaurus TCAD simulation tool is utilized to carry out the work.

2. Simulation

The high frequency (HF) C – V and I – V characteristics of the HfO_2 -based MOS device are simulated with and without ILs by Sentaurus TCAD software.⁸ The software tools solve

fundamental, physical and partial differential equations related to a device. The device is represented by a meshed finite element structure. Each node of the device has properties associated with it such as material type and doping concentration. The carrier concentration, current densities, electric field, generation and recombination rates are computed for each node. Electrodes are represented as areas on which voltages are applied. The device simulator solves the Poissons equation, the carrier continuity equation and other relevant equations. After solving the equations, the resulting electrical properties are extracted. The effect of substrate temperature, IL thickness and doping concentrations on the MOS characteristics is also studied. In all the cases, aluminum is used as the gate electrode. In this case, the TCAD models, used here, are adequate to simulate the device physics approximately at nanometer regime. Scattering inside the intrinsic device is treated by a simple Brooks Herring model giving a phenomenological description. This model can also capture the essential physics realistically. Enhanced Lombardi model is used for mobility that accounts for the mobility degradation due to IL and high- κ gate dielectrics. The simulation of C – V curve at a given frequency is based on the evaluation of differential capacitance associated with the interface traps when a small modulation of ac signal is superimposed on the dc gate voltage. The total capacitance of the MOS structure is a function of oxide capacitance, semiconductor capacitance and differential capacitance. The C – V characteristics are simulated at a frequency of 1 MHz by sweeping the gate voltage from the accumulation to the inversion condition through depletion.

In this work, three device structures namely D60 (HfO_2 6 nm-thick and no IL), D51 (HfO_2 of 5 nm and 1 nm SiO_2

Fig. 1. The mesh structure of HfO₂/Si MOS device.

layer as IL) and D42 (HfO₂ of 4 nm and SiO₂ of 2 nm) are used for simulation. ILs of different thicknesses have been taken here into consideration for their growth at the time of annealing during fabrication of MOS devices. The mesh structure of a device is shown in Fig. 1.

3. Results and Discussion

Figure 2 shows the HF $C-V$ curves for the high- κ gate dielectric with and without IL of SiO₂ where the total film thickness is kept as 6 nm. The curve “a” shows the variation of capacitance for D60 device, while curves “b” and “c” indicate the same for D51 and D42, respectively. It is evident that the device with no IL exhibits the highest accumulation capacitance. Since the IL is of a lower dielectric constant than that of HfO₂, a decrease in the capacitance is observed due to the decrease of the series capacitance with the increasing IL thickness. Actually, the effective dielectric constant is reduced due to an increase of the IL thickness that reduces the total structure capacitance. The variation in the slope of “b” and “c” curves indicates generation of interface traps due to the growth of the ILs.^{9,10} The shift in flatband voltage, V_{fb} , (shown in the inset) is mainly due to the substantial growth of interfacial oxide (SiO₂-rich layer) that increases with IL thickness.

Fig. 2. HF $C-V$ characteristics of HfO₂/Si MOS device (a: D60, b: D51, c: D42), inset shows normalized capacitance. Fig. 3. Temperature-dependent $C-V$ characteristics of the D51 and D42 MOS devices (inset shows the $C-V$ curve for D60 device). Direction of arrow indicates increasing temperature.

Temperature dependence of the $C-V$ characteristics of HfO₂/Si MOS structure with IL for D51 and D42 devices are shown in Fig. 3, whereas the inset shows the same for D60 device without IL. The simulations in all the cases are carried out at substrate temperatures of 25 °C, 50 °C, 75 °C and 100 °C, respectively. The temperatures 25 °C and 50 °C are considered as low temperature whereas the others are considered as high temperature. It is observed that the inversion capacitance increases slowly with the substrate temperature for D60 and D42, which is distinctly visible at 100 °C for both the cases whereas such phenomenon remains absent for D51 device. With the increase in substrate temperature, the thermal carrier generation takes place in the silicon substrate that becomes predominant in electron-hole pair generation. It should be noted that minority carrier generation time also increases with temperature; therefore, the variation of capacitance at high-frequency shows its low-frequency nature at higher substrate temperature. It is to note that no such effect of substrate temperature is observed for the D51 device. So, the presence of IL of 1 nm makes the device more reliable for its use at elevated temperature.¹¹

Figures 4 and 5 show the effect of doping concentrations of the substrate on the $C-V$ curves for the samples D60 and D51 at temperatures 300 K and 400 K, respectively. A stretch out of the curves and increase in the minimum capacitance are observed with increasing doping concentrations. The stretching is more pronounced for D51 sample. The effects are explained in terms of the depletion layer width and temperature-dependent behavior of n_i , the intrinsic carrier concentration of silicon. The maximum depletion width is inversely proportional to the square root of doping concentration and the capacitance is inversely proportional to depletion width. As a result, the minimum capacitance is directly proportional to doping concentration.

Fig. 4. HF C - V characteristics for D60 sample for two measured temperature (lower curves for 300 K and upper curves for 400 K) for three doping concentrations 10^{15} , 10^{16} and 10^{17} cm^{-3} , respectively. Direction of arrow indicates increasing doping concentration.

The leakage current characteristics of the MOS devices at room temperature are shown in Fig. 6. It is observed that in the presence of the IL, the leakage current increases quickly at lower voltage due to the unintentional IL growth in the device. In D60 device, a pre-breakdown condition is observed where the leakage current increases with gate voltage slowly and smoothly because charges begin to stack in the bulk high- κ to form a spot-connected breakdown path with a further evidence of quasi-breakdown process at higher gate voltage, which is due to the formation of a small number of connected paths.¹² Comparing the performances of D51 and D42 with

Fig. 5. HF C - V characteristics for D51 sample for two measured temperature (lower curves for 300 K and upper curves for 400 K) for three doping concentrations 10^{15} , 10^{16} and 10^{17} cm^{-3} , respectively. Direction of arrow indicates increasing doping concentration.

Fig. 6. Leakage current characteristics of the MOS devices.

D60 device, it is seen that presence of the IL degrades the insulating properties of the overall gate oxide. The higher leakage current is due to the presence of grain boundaries within the IL, where such grain boundaries provide leakage paths through the gate oxide layer.¹³ The spikes appearing at lower voltage range are due to the tunneling effect. The Pool-Frankel mechanism is responsible for conduction of current at higher gate voltage.¹⁴

The temperature-dependent leakage current with different ILs is plotted in Fig. 7. It appears that the leakage current shows spikes up to ~ 1.25 V at a substrate temperature of 25°C for D51 device. The number of spikes decreases at a temperature of 100°C . A ramp is found at about 1.25 V for both the temperatures and the current finally attains their respective saturation values. The leakage current for D42 appears only at a gate voltage of 1.75 V without any spikes. The current ramp starts at the same gate voltage for the

Fig. 7. Temperature-dependent I - V characteristics of the D51 and D42 MOS devices.

devices at temperatures of 25°C, 50°C, 75°C and 100°C. The saturation value of leakage currents for two devices, namely D51 and D42 at a temperature of 25°C, meets at ~ 11 V, whereas, the I - V characteristics for the devices at 100°C meets at ~ 5 V. It is evident from the above that the change in leakage current is more prominent at lower temperature for the devices with different IL thicknesses and there is no significant change in leakage current at higher substrate temperature. The electrons, tunneled through the SiO₂ IL, reach the SiO₂/HfO₂ interface. Defects, present at the IL and occupied energetic levels close to the bottom of the conduction band of HfO₂, participate in the conduction mechanism via a field- and trap-assisted electron trapping and detrapping process i.e., the Poole-Frenkel mechanism. For D51 sample, at $V_G < 1.25$ V, the Fermi level of the substrate is below the energy level of the trapping center of HfO₂. As a result, the electrons are not trapped by the trapping centers of HfO₂ and can be tunneled through the SiO₂/HfO₂ stack. Thus, the leakage current weakly depends on the substrate temperature and also produces some spikes. For $V_G > 1.25$ V, the Fermi level in the substrate lies above the energy level of the trapping center of HfO₂, and the electrons, injected into the HfO₂, can be trapped and detrapped by the defects. In this case, the Poole-Frenkel mechanism becomes the dominant charge transport mechanism and the current flowing through the structures strongly depends on the temperature.

4. Conclusion

Simulation of MOS devices by incorporating IL i.e., growth of IL at the time of deposition and/or annealing during MOS fabrication, shows that an ~ 1 nm-thin IL improves the device performance but a further increase in IL thickness causes degradation of the device quality. The I - V characteristics for all the samples further indicates that current ramps with voltage quickly at higher substrate temperature as well as with higher interfacial oxide thicknesses.

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