The Route for Ultra-High Recording Density Using Probe-Based Data Storage Device

Lei Wang*, Jing Wen, CiHui Yang, Shan Gai and YuanXiu Peng

*School of Information Engineering
Nanchang HangKong University
Nanchang 330063, P. R. China*

**LeiWang@nchu.edu.cn*

Received 2 June 2015

Accepted 16 July 2015

Published 2 September 2015

Phase-change probe memory using $\text{Ge}_2\text{Sb}_2\text{Te}_5$ has been considered as one of the promising candidates as next-generation data storage device due to its ultra-high density, low energy consumption, short access time and long retention time. In order to utmostly mimic the practical setup, and thus fully explore the potential of phase-change probe memory for 10 Tbit/in² target, some advanced modeling techniques that include threshold-switching, electrical contact resistance, thermal boundary resistance and crystal nucleation-growth, are introduced into the already-established electrothermal model to simulate the write and read performance of phase-change probe memory using an optimal media stack design. The resulting predictions clearly demonstrate the capability of phase-change probe memory to record 10 Tbit/in² density under pico Joule energy within micro second period.

Keywords: Tera bit; phase-change material; scanning probe; areal density.

1. Introduction

A drastic increase in the amount of information created and reproduced in digital form has been recently witnessed, resulting in a breakthrough of Zettabyte barrier in 2012 and a growth factor of 300 from 2005 to 2020.¹ This incomprehensive growth has vigorously triggered the development of storage areal density toward 10 Tbit/in² that is required to meet the storage demand for such ever-increasing global data.² Hard disk drive (HDD),^{3,4} optical disc drive (ODD),^{5,6} and Flash memory^{7,8} are currently three primary memory devices for mass storage applications. These three devices are

however facing stringent challenge to continue to increase storage capacity while lowering the cost per bit so as to satisfy the growing information demands in zettabytes that are estimated to be increasing at $\geq 50\%$ per year.^{9,10} As holding the dominant share of the storage market, HDD has exhibited several advantages including high data rate, short access time and relatively low cost per GB. Nevertheless, the most attractive attribute of HDD is its large capacity. Triggered by the inventions of the perpendicular recording and the tunneling magnetoresistance sensor, HDD has witnessed an areal density increase from 380 Gb/inch² in 2008 to 750 Gb/inch²

This is an open access article published by World Scientific Publishing and distributed under the terms of the Creative Commons Attribution (CC BY) 4.0 License, which permits use, distribution and reproduction in any medium, provided the original author(s) and source are credited.

in 2012,¹¹ which is accompanied with a cost decrease from \$0.272/GB to \$0.100/GB over the 2008–2012 time span.¹¹ In order to maintain such a majestic density augment, the magnetic bit size needs to be continuously scaled down. Unfortunately, there is a threshold grain volume existing, below which grain is likely to lose its thermal stability, also known as superparamagnetic effect. Due to the superparamagnetic effect, the perpendicular magnetic recording will approach its density limit in the near future, thereby necessitating the requirements for more innovative magnetic recording technologies. As the predecessor of the mass storage device, ODD has played an important role in the data storage history, particularly for music storing, due to its superiority over conventional HDD such as convenient removability, high data stability and long media life. The areal density offered by optical storage mainly depends on the size of laser spot focused on optical disc whose diameter is proportional to λ/NA , where λ is the wavelength of the laser beam and NA is the numerical aperture of the objective lens. It is natural to deduce that the areal density of ODD can be increased by either reducing the wavelength or increasing the numerical aperture, leading to the three generations of optical discs, i.e., compact disc (CD), digital versatile disc (DVD) and Blu-ray disc (BD). In addition to the write-once-read-many (WORM) ODD, the introduction of the phase-change layer into the optical recording technology has made re-writable (RW) ODD commercially available, delivering a series of well-known products such as CD-RW, DVD-RW, DVD+RW and BD-RE. In spite of these encouraging achievements, the capacity of optical disc has increased at a much slower rate during last 20 years than its rivals. To date, the maximum capacity that a single-sided optical disc can offer is approximately 30 GB,¹² while other storage devices have already achieved a TB capacity or more. Moreover, the fact that the cost per GB of an optical disc is around \$2.50 clearly suggested that optical disc is much more expensive than other competitive storage devices.¹³ To further extend the areal density of the ODD, a laser beam with a wavelength less than Blu-ray and NA higher than 0.85 is required. However, reducing the wavelength into ultraviolet regime is severely limited by current solid state laser technology and therefore may not be achieved very soon. Increasing NA usually accompanies with a high system sensitivity to dust and fingerprints and a

short depth of the focus.¹⁴ As a consequence, the wavelength of the recording laser beam and the NA of an objective lens are limited to 405 nm and 1 (in air), also known as diffraction limit. For this reason, the most common perspective with regard to the prospect of ODD is that it is gradually approaching to its demise. As the favorite replacement for conventional mass storage technologies, Flash memory has currently become an ubiquitous device for worldwide consumers and the growth rate of the storage capacity for Flash memory is even faster than the prediction of the Moore's Law due to its potential high capacity, fast access time and stable operation. In addition, if the number of electrons stored in Flash can be controlled precisely, the readout current can therefore be sensed in different levels (rather than pure "presence" or "absence"), resulting in the storage of two bits of information or more per memory cell without shrinking any feature size, known as multi-level technology. At present, the majority of the solid state drive (SSD) market has been governed by the NAND Flash, having higher density, lower cost, lower power consumption and faster programming performance. NAND Flash is designed at a low cost [(about US \$1/GByte in 2011 See Ref. 7) and the latest technology has allowed for a volume production of 64 Gb NAND Flash.¹⁵ To date, NAND Flash has been considered as a replacement for HDD, and NAND Flash-based SSD has already been adopted in personal computer and servers to substitute HDD.¹⁶ Although great achievements have been attained in Flash in terms of size reduction and cost lowering, Flash memory inevitably faces some scaling limits when further shrinking the cell size for higher density, primarily arising from the thickness of the tunnel oxide layer, the gate coupling ratio and the interference from the adjacent cells. As a consequence, the state of art NAND Flash is restricted to 20 nm node.⁷

As a result, a considerable research has been performed to develop new alternative memory technologies to replace or compete with the conventional approaches that have dominated the past so as to fulfil the need from both consumer and from the industry point of view.^{17–20} Phase-change probe memory, one such promising emerging storage technology, has recently gained enormous interest due to its ability to change the phase of the recording media within nanoscale region that can represent binary data. In phase-change probe memory, recording is realized by applying an

electrical potential via a conductive tip to switch the phase of the recording layer between highly resistive amorphous phase and highly conductive crystalline phase, and such a change on electrical resistivity between these two phases can be detected in the form of the readout current to achieve the readout process. The chalcogenide alloy such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST), has been extensively adopted for phase-change probe memory applications owing to its relative easiness for phase transformation, good stability and large reading contrast.^{21–24} Consequently, the integration of the superb characteristics of GST alloy as recording media together with the use of nanoscale conductive probe for recording equipment renders phase-change probe memory advantageous as a “universal” memory over other storage forms. First, it may be possible to use phase-change probe memory as cache memories. Although the access time of phase-change probe memory is not competitive with that of specific cache design technologies, it can have a competitive access time with respect to HDD (down to 1 ms, whereas state-of-the-art hard disks, turning at 15 000 RPM, reach 3 ms and are bulky) and are much less expensive than cache memory.²⁵ Such a low cost, decent access time associated with a high capacity allows for an improvement of mass storage performance under heavy traffic, particularly in massive server storage for online or grid computing. Furthermore, probe storage memory might be used in portable devices as a replacement of Flash. Although Flash still plays an essential role in the portable device market, it is subjected to the previously discussed scaling problem.²⁶ For probe storage, the bit size is not limited by lithographic fabrication. Most importantly, probe storage memory has a potential to achieve very high density mass storage in a small size with high performance, which might be able to satisfy the needs of the important archiving storage and backup markets. Table 1 compares the performances of the

probe-based memory with those of the three mainstream devices, i.e., HDD, ODD and NAND Flash.

In this case, in order to deeply understand the physical mechanisms involved in the use of phase-change probe memory, and thus accurately evaluate its potential to achieve 10 Tbit/in² target, it is very necessary to develop a physics-based comprehensive model to simulate the write and read performance of phase-change probe memory under an analogous condition to practical environment. It should be mentioned that the storage function of the probe-based memory can be theoretically accomplished by either forming crystalline phase inside the amorphous background (SET state) or vice versa (RESET state). To trigger the SET state, the temperature inside the amorphous phase needs to be heated above the glass transition temperature but below the melting point. To recover the amorphous phase to achieve RESET state, a high current pulse heats up the crystalline region to the melting temperature, followed by a rapid cooling that turns the undercooled molten material into the amorphous phase. However, the experimental writing of amorphous bits in a phase-change medium using electrical probe techniques has, to our knowledge, been reported only by one group of researchers (Tanaka’s group at Hokkaido University),²⁸ whereas there are numerous reports of the successful writing of crystalline bits in an amorphous matrix.^{29–31} This might imply that the writing of amorphous bits is experimentally difficult. Furthermore, it should be noted that in Tanaka’s case, the phase-change medium was protected from oxidation by being immersed in an inert liquid (3M, Fluorinert FC-43) and the writing tip contacted directly with the phase-change layer. Obviously, a liquid protective layer is not practicable for real storage systems. If a thin diamond-like carbon (DLC) capping layer is utilized for the practical system, the use of high current pulse would generate excessive temperature and a high

Table 1. Performance comparison between Probe-based memory and conventional mass storage devices.²⁷

Attribute	Probe	DVD	SATA-HDD	NAND
Density (Gb/sq.in.)	1000 to 10 000	>5	100–200	16
Capacity (GB)	2000 to 20 000 on 100 cm ²	4.7/9.4	600	64
Data Rate (MB/s)	>50 (512 levers, 1Mb/s/lever)	2.8–4	~100	~8
Access time	<1 ms	~150 ms	~10 ms	<0.1 ms
WO or RW	WO and RW	WO and RW	RW	RW
Lifetime (yr)	50	10–50	10	>10
Power(12 TByte system)	<5 W	~300 W	~5 kW	N/A

electrical field inside the overcoating layer during the writing of amorphous bits, thus causing extra power consumption. This may help to explain why so far no one has reported on the writing of amorphous bits in such practical stack designs. Therefore, in this paper we only focused on the writing of crystalline bits.

2. Model Geometry

The prerequisite for phase-change probe memory to yield 10 Tbit/in² is to find out an appropriate system architecture that is suitable for ultra-high density, short access time and low energy consumption. A typical phase-change probe memory shown in Fig. 1 usually consists of a recording tip and a media stack that constitutes a GST layer sandwiched by a capping layer and an under layer, which are deposited on substrate.

The capping layer can not only protect the GST layer from wear and corrosion, but also strongly influence the resulting electric field and temperature distribution inside the GST layer.³² A thin capping layer with high mechanical hardness, relatively large electrical conductivity and fairly low thermal conductivity is desired in order to generate sufficiently high temperature in GST layer for the required phase transformation while under low energy consumption. Under layer that acts mainly as a bottom electrode plays a minor role in determining the electric field and the required temperature for phase transformation than capping layer.^{32,33} In spite of this, an under layer with large electrical conductivity and low thermal conductivity is anticipated so as to reduce the writing power as well as overwhelming the heat dissipation through under layer toward substrate. A parametric study has been previously performed to establish the proper thickness and the characteristic parameters of the capping and under layer by taking into account aforementioned factors as well as the underlying

issues from practical fabrication process (e.g., electrical and thermal conductivities are usually inter-related, both of which depend on the layer thickness).^{32,34–38} According to this, the capping and under layer presented here make use of DLC and titanium nitride (TiN) with thickness, electrical conductivity and thermal conductivity of 2 nm, $100 \Omega^{-1}\text{m}^{-1}$, $0.2 \text{ Wm}^{-1}\text{K}^{-1}$ and of 40 nm, $0.5 \times 10^7 \Omega^{-1}\text{m}^{-1}$, $12 \text{ Wm}^{-1}\text{K}^{-1}$, respectively. The GST layer employed as the recording media has a remarkable effect on the required writing energy for phase transformation ascribed to the so-called threshold switching effect which exhibits a field dependence.^{39–41} The thickness of GST layer is thereby required to be thin in order to provide high electric field for a given low writing pulse. The thickness of GST layer used here is considered as 10 nm, which is a typical thickness for phase-change probe memory.^{32,33,42}

Regarding tip design, one of the most attractive features of phase-change probe memory is to allow the usage of a smoother tip than other probe techniques requiring a very sharp tip, since the current is passing through the Hertzian contact area between tip and sample.⁴³ Therefore, the tip does not need to be physically sharp, but merely electrically sharp (small electrical contact area). This could alleviate tip tribology and wear issues. Based on this idea, a novel silicon dioxide (SiO₂) encapsulated silicon (Si) tip with platinum silicide (PtSi) at the tip apex has been proposed, as shown in Fig. 2.⁴⁴

Forming PtSi at the tip apex can significantly improve the conduction and wear properties of the conductive tip, as PtSi provides a superior anti-wear characteristic as well as very high electrical conductivity ($3.3 \times 10^6 \Omega^{-1}\text{m}^{-1}$). Moreover, the use of the dielectric encapsulation can increase the physical diameter of the tip and thus contributes to lower

Fig. 1. Schematic of phase-change probe memory.

Fig. 2. Scanning electron micrograph of PtSi tip with SiO₂ encapsulation. Taken from Ref. 44.

levels of wear due to the reduced pressure between tip and sample. It was found that the electrical conductivity of such an encapsulated tip was sustained for at least 2.5 m of sliding on an amorphous carbon, well addressing the issue of long-term conduction and mechanical stability of tip apexes for use in conducting probe technologies.⁴⁴ Due to the above reasons, such an encapsulation tip is utilized here as the recording means. The combination of aforementioned considerations gives rise to the optimal architecture of the phase-change probe system, as illustrated in Fig 1.

3. Advanced Modeling Techniques

The physical mechanisms that determine the write and read performances of phase-change probe memory involve electrical, thermal and phase-transformation processes. A pseudo-3D computational model for all such processes using Finite-element method was previously introduced by simultaneously solving the (time-resolved) Laplace, heat conduction and Johnson–Avrami–Kolmogorov (JMAK) equations.^{32,34,45–47} However, there are some severe drawbacks existing for this model, which consequently impair its physical credibility. The electrical conductivity of amorphous GST media in the model was assumed to be electric field-dependent exclusively, while this assumption may be too simple to provide an accurate description on the threshold switching effect mainly relying on transport properties of carriers.^{48,49} In addition, an ideal interface conditions were assumed in the previous simulations, i.e., electrical contact resistance and thermal boundary resistance were both considered as zero. This is obviously not realistic in practice due to existence of finite interfacial resistance in real systems. More importantly, JMAK theory for the description of phase-transformation process in the previous model cannot be used to predict the heterogeneous nucleation that has been experimentally observed for GST media.^{50,51} Therefore, it is essential to develop advanced modeling techniques, to circumvent the above limitations, and thus to provide a physically realistic prediction concerning the potential of phase-change probe memory for 10 Tbit/in².

3.1. Threshold switching modeling

Note that real semiconductor materials usually have defects occurring within the solid. These defects

divide the forbidden-energy band into numerous discrete electronic energy states, also known as traps. As the chalcogenide in amorphous phase can be regarded as a semiconductor with many defects, trap would play an important role in determining the transport mechanism of charged carriers in amorphous chalcogenides. In addition to the traps, defects and interface traps may also affect the electrical transport behavior of amorphous chalcogenide to some extent. Amorphous materials like chalcogenide glasses are characterized by charged defective states, a.k.a. valence alternation pairs (VAPs), which act as recombination centers. Positive defects can be neutralized by acquiring an electron, whereas negative centers can combine with holes. Electrons and holes are generated via impact ionization, so that extra pairs of carriers generated along the material can interact with VAPs. When the electrical field reaches a critical value, a great concentration of holes is generated near the anode and the material can switch to the ON state. The holes neutralize negative traps in the bulk, leaving there and excess of positive defects. Then, according to the kinetics of equilibrium, these defects react with electrons (from the cathode), leaving an excess of negative charges, that are compensated by positive charges from the anode. When the new equilibrium is established, since the majority of VAPs are now neutral, a conductive filament where electrons can transit without being trapped is created, and the conductivity is greatly enhanced. On the other hand, interface states, characterized by a density state, are able to capture charge carriers and, hence, become charged. These additional charges introduced into the system are distributed along the channel and perturb the electrostatics of the device. Furthermore, they act as additional scattering centers thereby degrading the readout current.⁵²

The writing current under the threshold switching regime based on the trap-limited transport theory has recently been reported as:⁴⁸

$$I = 2qA(N_{T1} + N_{T2})\frac{\Delta z}{\tau_0}e^{-\frac{E_C - E_F}{kT}} \times \sinh\left(\frac{qV_A \Delta z}{k_B T 2u_a}\right)(1 + \gamma), \quad (1)$$

where N_{T1} is the concentration of a deep traps at energy E_F for Fermi level, N_{T2} is the concentration of a shallow traps at energy E_C for the conduction

band, A is the cross-sectional area of chalcogenide device, τ_0 is the attempt-to-escape time for the trapped carrier, V_A is the applied voltage, u_a is the thickness of the chalcogenide device, q is the unit charge, Δz is the intertrap distance, k_B is the Boltzmann constant, T is the temperature and γ is a nonequilibrium term, written as:

$$\gamma = \frac{N_{T1}}{N_{T1} + N_{T2}} \frac{\tau_n}{\tau_0} e^{-B_{12}u_a/V_A} e^{-(E_{T1}-E_{T2})/kT}, \quad (2)$$

where τ_n is the effective time for electron relaxation from shallow to deep traps, E_{T1} is the energy aligned with Fermi level, E_{T2} is the energy level close to the conduction band, and B_{12} is given by:

$$B_{12} = \frac{4(2m)^{1/2}(E_{T2} - E_{T1})^{3/2}}{3q\hbar}, \quad (3)$$

where m is the effective electron mass and $\hbar$ is the Planck constant divided by 2π .

In order to include threshold switching effect, it is viable to derive the electrical conductivity of the amorphous GST from the above writing current, since the electrical conductivity is the sole parameter required to solve the Laplace equation that is responsible for electrical process. Based on Ohm's law, the electrical conductivity of a specific finite element inside the GST layer is given by:

$$\frac{u_{\text{element}}}{\sigma \cdot S_{\text{element}}} = \frac{V_{\text{element}}}{I_{\text{element}}}, \quad (4)$$

where u_{element} and S_{element} are the thickness and the cross section of the finite element, respectively, V_{element} and I_{element} are the voltage and current across the finite element, respectively, and σ is the electrical conductivity of the finite element.

Rewriting Eq. (1) as

$$I_{\text{element}} = 2qS_{\text{element}}(N_{T1} + N_{T2}) \frac{\Delta z}{\tau_0} e^{-\frac{E_C-E_F}{kT}} \times \sinh\left(\frac{qV_{\text{element}}}{kT} \frac{\Delta z}{2u_{\text{element}}}\right) (1 + \gamma), \quad (5)$$

Substituting Eq. (5) for I_{element} in Eq. (4), resulting in:

$$\sigma = \frac{u_{\text{element}}}{V_{\text{element}}} \cdot 2q(N_{T1} + N_{T2}) \frac{\Delta z}{\tau_0} e^{-\frac{E_C-E_F}{kT}} \times \sinh\left(\frac{qV_{\text{element}}}{kT} \frac{\Delta z}{2u_{\text{element}}}\right) (1 + \gamma). \quad (6)$$

It is obvious that $V_{\text{element}}/u_{\text{element}}$ is equal to the electric field E across the finite element. Therefore,

Eq. (6) can be rewritten as:

$$\sigma = E^{-1} \cdot 2q(N_{T1} + N_{T2}) \frac{\Delta z}{\tau_0} e^{-\frac{E_C-E_F}{kT}} \times \sinh\left(\frac{qE}{kT} \frac{\Delta z}{2}\right) (1 + \gamma), \quad (7)$$

where N_{T1} and N_{T2} are both considered to be 10^{25} m^{-3} , $E_C - E_F$ is taken as 0.35 eV, τ_0 is 10^{-15} s , Δz is $5 \times 10^{-9} \text{ m}$, q is $1.6 \times 10^{-19} \text{ C}$ and k is $1.38 \times 10^{-23} \text{ J/K}$.

Therefore, in order to better describe the threshold switching behavior, the electrical conductivity of amorphous GST in the form of Eq. (7) was introduced into the Laplace equation to replace the previous field-dependent one.

3.2. Interfacial resistance modeling

The influence of the interfacial resistance including electrical contact resistance and thermal boundary resistance on the write and read performances of phase-change probe memory were ignored in previous simulations, whereas they could have a significant effect on the temperature distribution within the phase-change device as well as the written mark size and shape for a given writing pulse. It should be noted that for practical operation, tip can penetrate a small distance into the sample due to the applied loading force, as shown in Fig. 3.

Such an indentation, H_{defl} , can be written as a function of the radius (r) of curvature at the apex of the tip, and the loading force F , given by:⁵³

$$H_{\text{defl}} = \left(\frac{9F^2}{16rE^*} \right)^{\frac{1}{3}}, \quad (8)$$

where E^* is the equivalent Young's modulus of elasticity, defined as:

$$\frac{1}{E^*} = \frac{1 - \nu_1^2}{E_1} + \frac{1 - \nu_2^2}{E_2}, \quad (9)$$

Fig. 3. Schematic of tip-sample interface for a loading force.

where E_1 and E_2 are the elastic modulus of the tip and the sample, respectively, and ν_1 , ν_2 are the corresponding Poisson's ratios. In this case, the contact radius, r_{con} is calculated by:

$$r_{\text{con}} = \left(r^2 - (r - H_{\text{defl}}^{\frac{1}{3}})^2 \right)^{\frac{1}{2}}, \quad (10)$$

The electrical contact resistance can thus be estimated as a function of the contact surface resistivities and the radius of the contact area, resulting in:⁵⁴

$$R_{\text{contact}} = \frac{\rho_{\text{tip}} + \rho_{\text{sample}}}{4r_{\text{con}}}, \quad (11)$$

where ρ_{tip} and ρ_{sample} are the resistivities of the tip and sample (capping layer in this case), respectively. According to this expression, the electrical contact resistance calculated here is approximately equal to 80 k Ω for a tip force of 300 nN (typical for that applied during writing) and for $\rho_{\text{sample}} = 0.01 \Omega\text{m}$ and $\rho_{\text{tip}} = 0.3 \times 10^{-6} \Omega\text{m}$ with an effective Young's modulus of 20.2 GPa.⁵⁵

In contrast to electrical contact resistance, the thermal boundary resistance between GST media and different electrode materials have been experimentally established.^{56–59} The values of thermal boundary resistance in the simulations presented here are $2.5 \times 10^{-8} \text{ m}^2\text{KW}^{-1}$ for DLC/GST interface, and $1.8 \times 10^{-8} \text{ m}^2\text{KW}^{-1}$ for GST/TiN interface, corresponding to the experimental measurements.^{56,57}

3.3. Crystal nucleation-growth modeling

The crystallization behavior of GST media in previous simulations was interpreted by JMAK theory that is only applicable to homogenous nucleation,⁶⁰ i.e., nucleation occurs everywhere at the same rate. However, this is not the case for GST media whose nucleation can occur at some preferential sites such as surfaces, interfaces and impurities, known as heterogeneous nucleation. Therefore, toward a better understanding of the phase-change process where heterogeneous nucleation may occur, the crystallization behavior of GST media is evaluated here based on the classical nucleation-growth theory rather than the JMAK model.

In terms of classical nucleation-growth theory, the homogeneous and heterogeneous nucleation rates can be written as:⁶¹

$$I_{\text{nuc}}^{\text{hom}} = \alpha \exp(-E_{\text{an}}/k_B T) \exp(-\Delta G_C/kT) \quad (12)$$

$$I_{\text{nuc}}^{\text{het}} = \beta \exp(-E_{\text{an}}/k_B T) \exp(-\Delta G_C f(\theta)/kT) \quad (13)$$

where α and β are the prefactors, E_{an} is the activation energy for nucleation, T is the temperature, k_B is Boltzmann constant, $f(\theta)$ is a shape factor and ΔG_C is the excess free energy for the formation of (energetically) stable crystal nuclei, given by

$$\Delta G_C = 16\pi\delta^3/3\Delta g^2, \quad (14)$$

where δ is the interfacial energy, and Δg is the Gibbs free energy difference between the crystal and the supercooled liquid, given by

$$\Delta g = \Delta H(T_m - T)/T_m, \quad (15)$$

where T_m is the melting temperature and ΔH is the enthalpy of fusion. Once the stable nuclei are formed, they can subsequently grow at a velocity of V_g , calculated by⁶²

$$V_g = V_0 \exp(-E_{\text{ag}}/k_B T) (1 - \exp(-\Delta g'/k_B T)), \quad (16)$$

where V_0 is a temperature dependent pre-factor, E_{ag} is the activation energy for growth, and $\Delta g'$ is the free energy difference per atom between the amorphous and crystalline phases, with other terms as mentioned above.

The simulation procedure is illustrated in Fig. 4. The GST layer to be simulated is divided into an array of square tiles with the dimension 1 nm $\times$ 1 nm, corresponding approximately to the minimum room temperature stable nucleus size in GST. It should be noted that in reality the dimension of the critical nucleus has exhibited a temperature-dependent property. However, it would be very difficult to introduce such a characteristic into the simulation, as the model geometry needs to be defined before the onset of the simulation for any finite element software package. In this case, in order to reduce the model complexity, the size of each critical nucleus is determined by room temperature only in this simulation. At each time step of simulation, both

Fig. 4. Simulation strategy for the developed nucleation-growth model.

Table 2. Numerical values for the nucleation-growth model.

Symbol	Value	Unit
α	1×10^{56}	$1/\text{m}^3\text{s}$
β	7×10^{46}	$1/\text{m}^2\text{s}$
E_{an}	2.6	eV
E_{ag}	2.6	eV
ΔH	1121	J/cm^3
T_m	893	K
δ	0.1	J/m^2

Laplace equation and heat conduction equation are first solved simultaneously to result in the temperature in each tile, which is used to calculate the nucleation probability. It should be noted that homogeneous nucleation probability that is responsible for the bulk GST crystallization is calculated by multiplying the nucleation rate in Eq. (12) by the time interval and the (notional) volume of a tile, while heterogeneous nucleation rate accounts for the GST crystallization at DLC/GST and GST/TiN interfaces is given by multiplying the nucleation rate in Eq. (13) by the time interval and the (notional) surface area of a tile. Once nuclei are formed, they can subsequently undergo a growth process, which can be simulated by calculating the growth radius that is given by the product of the growth velocity in Eq. (16) and the time interval. $f(\theta)$ is equal to 0.6, and V_0 is equal to $\varepsilon \exp(-0.8/(1 - T/T_m)) \text{ ms}^{-1}$ with ε equal to 3.9×10^{19} , while other relevant parameters are shown in Table 2.

4. Results and Discussions

Based on the results discussed so far, it is illuminating to introduce all of the advanced modeling techniques presented above into the previous electrothermal simulation, to pursue a more realistic result, and also to investigate the feasibility of using the optimal stack shown in Fig. 1 for storage density of 10 Tbit/inch² (bit diameter is required to be around 10 nm), such storage densities being undoubtedly necessary in the not too distant future. Although this writing simulation is still performed in 2D with circular symmetry in order to reduce the computational time, the previous JMAK model and field-dependent electrical conductivity of amorphous GST have been replaced with the developed nucleation-growth model and a more physically

Fig. 5. 10 Tbit/in² recording using the design media stack and advanced modeling techniques.

realistic conductivity based on trap-limited-transport theory to take into account the heterogeneous nucleation and threshold switching effect. Besides, the electrical contact resistance has been added to the tip/DLC interface, and the thermal boundary resistance has been introduced to the DLC/GST and GST/TiN interfaces to mimic a practical interface condition.

Figure 5 shows the resultant crystalline bit formed by an application of a 6 V pulse of 100 ns. It is revealed in Fig. 6 that, using a 6 V pulse of 100 ns is able to generate a spherically shaped bit with a diameter of around 10 nm, satisfying the requirement for the areal density of 10 Tbit/inch². Moreover, the writing power for such a bit is around 0.016 mW, resulting in a writing energy per bit of 1.6 pJ. As a result, the total writing energy required for using 100 and 1000 tips (i.e., a typical array of AFM cantilevers consisting of 32 × 32) in parallel are 0.16 nJ and 1.6 nJ respectively, which is much lower than any other probe-based memories.^{63–65} Experimental recording experiments were also carried out using this same media structure and PtSi tip design

Fig. 6. The resulting I - V curve.

to verify the physical reality of the developed model. It was found that the bit is around 12 nm in diameter and the energy needed to record such a bit is only 2 pJ in the experimental case, fitting our simulation well. Most importantly, the crystalline bit shown in Fig. 5 is reported to be thermodynamically stable at the temperature below 550°C, demonstrating its long retention time at archival temperature.³²

In addition to the written bit, the resulting I - V curve and the temperature distribution inside the system at the end of the rising edge of the applied pulse are also shown in Figs. 6 and 7, respectively. As can be seen from Fig. 6, the writing current initially remains in the sub-threshold regime even if the writing voltage increases. Once the voltage reaches the threshold level, a sudden increase on the writing current was observed due to the significant drop in the resistance of the amorphous phase. Based on Fig. 6, the threshold voltage is around 4.5 V and in the case the threshold field can be calculated using threshold voltage/GST thickness, which is approximately equal to 4.5×10^8 V/m. This value is very close to the previously reported counterparts,³² further demonstrating the physical reality of the designed model. For temperature contour, it can be seen from Fig. 7 that the maximum temperature is formed near the GST/capping interface. This is expected since the majority of Joule heat is accumulated in this region due to the fairly low thermal conductivity of the capping layer, generating a higher temperature than elsewhere. Besides, the comparison between Figs. 5 and 7 reveal a fact that

Fig. 7. Temperature distribution at the end of the rising edge of the pulse.

Fig. 8. The simulated ISI effect with a tip movement of 25 nm.

the size of the crystalline bit is approximately the same as the temperature contour region greater than 400°C. This is because 400°C is the critical point that is required to achieve crystallization during the period of hundreds of nanoseconds.

It should be however noted that the decrease of the bit distance may exacerbate the inter-symbol effect (ISI) induced from the influence of the previously written bit on the bit that is being written or read. In order to investigate the ISI effect, the previously introduced electrothermal model has been re-run with a tip movement of 25 nm from the first recording position to perform the second recording, giving rise to Fig. 8. In this case, the results attained from the first recording simulation are considered as the initial values of the second simulation, and other writing parameters used to produce Fig. 8 are as for Fig. 5. As can be seen from Fig. 8, a relatively severe ISI effect has been found with a tip movement of 25 nm, as the shape of the second written bit is strongly affected by the first recorded bit (i.e., the second bit exhibits a “tail” pointing toward the first bit). This is expected since the writing current would preferentially flow into the previously recorded bit due to its much higher electrical conductivity than the surrounding amorphous background. It can be therefore concluded that tip should at least move more than 25 nm to avoid interference caused by the previously written bits.

In addition, a simple 2D readout model was utilized to plot the isolated bit response of the written bit shown in Fig. 5 by solving the Laplace equation to attain the readout current along with the tip movement in terms of the system structure in Fig. 1. The result shown in Fig. 9 reveals that such a written crystalline bit with amorphous background is able to give a usable readout signal with the full width half magnitude (FWHM) of around 20 nm width. Although the FWHM of this readout pulse is

Fig. 9. The isolated bit response of the written bit for a given readout potential of 1 V.

slightly larger than the bit itself, this is to be expected since the readout signal essentially results from a convolution of this tip (which itself is 10 nm in diameter) and the recorded bit. This is a similar situation to other storage systems, such as magnetic hard disks, where the FWHM of the readout pulse is wider than the recorded magnetic transition itself due to the finite size of the readout head (and the head-medium spacing).⁶⁶ Hence, it is to be expected that the design of a suitable readout channel for the bit response of Fig. 9 should be relatively straightforward. It should also be pointed out that the configuration with reading crystalline bit from amorphous background exhibits a higher readout contrast, i.e., $I_{\max} - I_{\min} / 0_{\max} + I_{\min}$ ($I_{\max}$ and $I_{\min}$ are the maximum and minimum readout currents, respectively), than reading amorphous bit from crystalline background. Another reason to avoid reading amorphous bit from crystalline background is because, considering that the electrical conductivity of the capping layer is higher than the amorphous bit, the readout current may bypass the amorphous bit and thus flow into the surrounding crystalline background via the capping layer. In this case, it would be very difficult to distinguish the amorphous bit from the surrounding crystalline background, causing readout error. Therefore, as long as the adopted readout voltage is well below the writing voltage to suppress the re-crystallization effect of the surrounding amorphous background (in this case, readout voltage is chosen to be 1 V, much lower than the writing voltage), the reading of crystalline bit from amorphous background exhibits a better readout behavior than reading amorphous bit from the crystalline background. Another factor

that may greatly affect the readout current is the scanning speed of the probe tip. If the tip is scanning at a relatively fast speed and the readout pulse can last up to the order of the μs scale, there might be a displacement between the actual position of the tip and its expected position at the end of the readout pulse. Therefore, the maximum magnitude of the readout current and the FWHM width for a tip with a fast scanning speed will be different from that with a slow scanning speed, as the tip may not be entirely overlapping with the bit that is being read. According to our equipment, the scanning speed of the probe tip is around 1 mms^{-1} , which is also the scanning speed adopted in Fig. 9. Consequently, the tip only moves 0.1 nm during a pulse of 100 ns. This would allow for a clear distinction on the readout currents between the crystalline bit and the amorphous background.

There is no doubt that single probes are relatively slow in writing and retrieving data, and in this case the spot dimension may strongly affect the read speed. However, high data rates are possible by operating large arrays of probes in parallel, with each probe performing read, write and erase operations on an individual storage field. As a consequence, the adverse influence of spot dimension on read speed would be aggressively attenuated. Therefore, based on such a simulation, it can be inferred that phase-change probe memory has the potential to meet the continuously growing demand for low power consumption, and high areal density data storage. It should be likewise emphasized that in spite of these promising results, probe-based phase-change memory still remains in laboratory level at present. This is because its writing/reading mechanisms are strongly related to the electrothermal process, and in this case the resulting density can be influenced by many factors, such as electrical/thermal properties of the recording media, tip diameter, tip wear and coating layers. Therefore, it may not be possible for probe-based phase-change memory to replace HDD or Flash as the mainstream mass storage devices in the near future before the correlated physical principles are well understood. As a consequence, in order to speed up the commercialization of probe-based phase-change memory, a thorough understanding on the electrical/thermal conduction mechanism of phase-change materials for probe applications is urgently required, giving rise to the motivation of this paper.

5. Conclusions

The potential of phase-change probe memory for 10 Tbit/in² is investigated through a combination of previous electrothermal simulation with some advanced modeling techniques to overcome the model limitations and thus to more closely mimic the practical setup. The previous empirical model for the electrical conductivity of amorphous GST is replaced with a more analytical one to give a more accurate and physically realistic description of threshold switching. The ideal interface condition in previous simulations is replaced with a mechanical model allowing for the calculation of electrical contact resistance between tip and capping layer, and an introduction of thermal boundary resistance between GST layer and capping/under layer. In addition, a crystallization model using classical nucleation-growth theory is developed to take into account both homogeneous and heterogeneous nucleations instead of the previous JMAK model can only tackle homogeneous nucleation. Introducing these modeling techniques into the previous electrothermal simulation using the designed memory architecture clearly demonstrates the feasibility of achieving an areal density of 10 Tbit/in² using phase-change probe memory.

Acknowledgments

The authors acknowledge the financial supports of the National Natural Science Foundation of China (Grant No. 61201439, 61202319) and the Educational Bureau of JiangXi Province (Grant No. GJJ13487, GJJ14540). The authors would also like to thank Prof C. D. Wright, Dr M. M. Aziz and Dr K. Kohary at University of Exeter for technical discussions on media stack designs, and Dr H. Bhaskaran at University of Oxford for technical discussions on tip design.

References

1. L. Wang, C. H. Yang, J. Wen, S. Gai and Y. X. Peng, *J. Mater. Sci. Mater. Electron.*, **26**, 4618 (2015).
2. K.-S. Park, Y.-P. Park and N.-C. Park, *IEEE Trans. Magn.*, **47**, 539 (2011).
3. X. B. Wang, K. Z. Gao, H. Zhou, A. Itagi, M. Seigler and E. Gage, *IEEE Trans. Magn.*, **49**, 686 (2013).
4. I. Iwasaki, *J. Magn. Magn. Mater.*, **324**, 244 (2012).
5. D. C. Koide, T. Kajiyama, H. Tokumaru, Y. Takano, Y. Nabata, T. Ogata, T. Miyazaki and K. Ohishi, *Jpn. J. Appl. Phys.*, **51**, 08JA04 (2011).
6. G. Overton, *Laser Focus World*, **48**, 39 (2012).
7. C. Y. Lu, *J. Nanosci. Nanotechnol.*, **12**, 7604 (2012).
8. S. K. Lai, *J. Nanosci. Nanotechnol.*, **12**, 7597 (2012).
9. L. Wang and S. Gai, *Contemp. Phys.*, **55**, 75 (2014).
10. L. Wang, C. D. Wright, P. Shah, M. M. Aziz, C.-H. Yang and G.-W. Yang, *Mater. Lett.*, **112**, 51 (2013).
11. H. Wang, H. B. Zhao, T. Rahman, Y. Isowaki, Y. Kamata, T. Maeda, H. Hieda, A. Kikitsu and J.-P. Wang, *IEEE Trans. Magn.*, **49**, 707 (2013).
12. J.-H. Kim, S.-H. Lee and J.-J. Seo, *J. Mod. Optic.*, **59**, 943 (2012).
13. A. Badalyan, R. Hovsepyan, V. Mekhitarian, P. Mantashyan and R. Drampyan, *Proc. SPIE.*, **7996**, 7996 (2011).
14. H. J. Borg, *J. Magn. Magn. Mater.*, **193**, 519 (1999).
15. K. Kanda, N. Shibata, T. Hisada, K. Isobe, M. Sato, Y. Shimizu and R. Yamashita, *IEEE J. Solid-State Circuits*, **48**, 159 (2013).
16. F. Yoshihisa, *Jpn. J. Appl. Phys.*, **52**, 040001 (2013).
17. T. W. McDaniel, *J. Appl. Phys.*, **112**, 093920 (2012).
18. M.-F. Hung, Y.-C. Wu and J.-H. Chen, *Appl. Phys. Lett.*, **100**, 052107 (2012).
19. J.-M. Hu, Z. Li, L. Q. Chen and C. W. Nan, *Nat. Commun.*, **2**, 1 (2011).
20. C. D. Wright, M. M. Aziz, P. Shah and L. Wang, *Curr. Appl. Phys.*, **11**, e104 (2011).
21. W. Gawelda, J. Siegel, C. N. Afonso, C. Plausinaitiene, A. Abrutis and C. Wiemer, *J. Appl. Phys.*, **109**, 123102 (2011).
22. Y. Liu, M. M. Aziz, A. Shalini, C. D. Wright and R. J. Hicken, *J. Appl. Phys.*, **112**, 123526 (2012).
23. T. S. Boscke, J. Muller, D. Brauhuis, U. Schroder and U. Bottger, *Appl. Phys. Lett.*, **99**, 102903 (2011).
24. M. Wuttig and N. Yamada, *Nature*, **6**, 824 (2007).
25. S. J. Hudgens, *J. Non-Cryst. Solid*, **354**, 2748 (2008).
26. S. K. Lai, *IBM. J. Res. Dev.*, **52**, 529 (2008).
27. L. Wang, C. D. Wright, M. M. Aziz, C. H. Yang and G. W. Yang, *Electron Mater. Letts.*, **10**, 1045 (2014).
28. K. Tanaka, *J. Non-Cryst. Solid*, **353**, 1899 (2007).
29. H. Satoh, K. Sugawara and K. Tanaka, *J. Appl. Phys.*, **99**, 024306 (2006).
30. H. J. Kim, S. K. Choi, S. H. Kang and K. H. Oh, *Appl. Phys. Lett.*, **90**, 083103 (2007).
31. C. D. Wright, M. Marilyn, M. M. Aziz, S. Senkader and W. Yu, *Proc. MRS.*, **803**, 61 (2004).
32. C. D. Wright, M. Marilyn and M. M. Aziz, *IEEE Trans. Nanotechnol.*, **5**, 50 (2006).
33. S. Gidon, O. Lemonnier, B. Rolland, O. Bichet and O. Dressler, *Appl. Phys. Lett.*, **85**, 6392 (2004).

34. C. D. Wright, L. Wang, P. Shah, M. M. Aziz, E. Varesi, R. Bez, M. Moroni and F. Cazzaniga, *IEEE Trans. Nanotechnol.* **10**, 900 (2011).
35. A. A. Balandin, M. Shamsa, W. L. Liu, C. Casiraghi and A. C. Ferrari, *Appl. Phys. Lett.* **93**, 043115 (2008).
36. M. Shama, W. L. Liu, A. A. Balandin, C. Casiraghi, W. I. Milne and A. C. Ferrari, *Appl. Phys. Lett.* **89**, 161921 (2006).
37. J. Robertson, *Mater. Sci. Eng. R* **37**, 129 (2002).
38. J. Hone, M. C. Llaguno, N. M. Nemes, J. T. Johnson, J. E. Fischer, D. A. Walters, M. J. Casavant, J. Schmidt and R. E. Smalley *Appl. Phys. Lett.* **77**, 666 (2000).
39. D. Adler, H. K. Henisch and N. Mott, *Rev. Mod. Phys.* **50**, 209 (1978).
40. D. Adler, M. S. Shur, M. Silver and S. R. Ovshinsky, *J. Appl. Phys.* **51**, 3289 (1980).
41. A. Redaelli, A. Pirovano, A. Benvenuti and A. L. Lacaita, *J. Appl. Phys.* **103**, 111101 (2008).
42. H. Bhaskaran, A. Sebastian, A. Pauza, H. Pozidis and M. Despont, *Rev. Sci. Instrum.* **80**, 083701 (2009).
43. H. Bhaskaran, B. Gotsmann, A. Sebastian, U. Drechsler, M. A. Lantz, M. Despont, P. Jaroenapibal, R. W. Carpick, Y. Chen and K. Sridharan, *Nat. Nanotechnol.* **5**, 181 (2010).
44. H. Bhaskaran, A. Sebastian and M. Despont, *IEEE Trans. Nanotechnol.* **8**, 128 (2009).
45. C. D. Wright, P. Shah, L. Wang, M. M. Aziz, A. Sebastian and H. Pozidis, *Appl. Phys. Lett.* **97**, 173104 (2010).
46. M. M. Aziz and C. D. Wright, *J. Appl. Phys.* **90**, 034301 (2006).
47. M. M. Aziz and C. D. Wright, *J. Appl. Phys.* **97**, 103537 (2005).
48. D. Ielmini and Y.-G. Zhang, *J. Appl. Phys.* **102**, 054517 (2007).
49. D. Ielmini, *Phys. Rev. B* **78**, 035308 (2008).
50. J. A. Kalb, F. Spaepen and M. Wuttig, *J. Appl. Phys.* **98**, 054910 (2005).
51. J. A. Kalb, F. Spaepen and M. Wuttig, *Appl. Phys. Lett.* **84**, 5240 (2004).
52. Pandian, Phase-change thin films: resistance switching and isothermal crystallization studies, Ph.D Thesis, Mathematics and Natural Sciences, University of Groningen, Groningen, Netherlands (2008).
53. H. Lo and J. A. Bain, Effect of high current density at nanoscale point contacts, in *Proc. Symp. on Micro/Nanoscale Heat Transfer*, Taiwan, 2008, P. 1 Taiwan (2008).
54. B. Bhushan, *Wear* **259**, 1507 (2005).
55. S. Cho, I. Chasiotis, T. A. Friedmann and J. P. Sullivan, *J. Micromech. Microeng.* **15**, 728 (2005).
56. J. P. Reifenberg, K.-W. Chang, M. A. Panzer, S. Kim, J. A. Rowlette, M. Asheghi, P. H.-S. Wong and K. E. Goodson, *IEEE Electron Device Lett.* **31**, 56 (2010).
57. F. Xiong, A. Liao and E. Pop, *Appl. Phys. Lett.* **95**, 243103 (2009).
58. J. L. Battaglia, A. Kusiak, V. Schick, A. Cappella, C. Wiemer, M. Longo and E. Varesi, *J. Appl. Phys.* **107**, 044314 (2010).
59. J. P. Reifenberg, M. A. Panzer, S.-B. Kim, A. M. Gibby, Y. Zhang, S. Wong, P. H.-S. Wong, E. Pop and E. Goodson, *Appl. Phys. Lett.* **91**, 111904 (2007).
60. S. Senkader and C. D. Wright *J. Appl. Phys.* **95**, 504 (2004).
61. D.-H. Kim, F. Merget, M. Forst and H. Kurz, *J. Appl. Phys.* **101**, 064512 (2007).
62. C. B. Peng, L. Cheng and M. Mansuripur, *J. Appl. Phys.* **82**, 4183 (1997).
63. P. Vettiger, G. Cross, M. Despont, U. Drechsler, U. Durig, B. Gotsmann, W. Haberle, M. A. Lantz, H. E. Rothuizen, R. Stutz and G. K. Binnig, *IEEE Trans. Nanotechnol.* **1**, 39 (2002).
64. Y. Cho, S. Hashimoto, N. Odagawa, K. Tanaka and Y. Hiranaga, *Nanotechnology* **17**, 137 (2006).
65. L. Zhang, J. A. Bain and J. G. Zhu, *J. Magn. Magn. Mater.* **305**, 16 (2006).
66. G. C. Han, J. J. Qiu, L. Wang, W. K. Yeo and C. C. Wang, *IEEE Trans. Magn.* **46**, 709 (2010).