Analysis of Phase Noise in 28 nm CMOS LC Oscillator Differential Topologies: Armstrong, Colpitts, Hartley and Common-Source Cross-Coupled Pair*

Ilias Chlis^{†,‡,§}, Domenico Pepe^{†,¶} and Domenico Zito^{†,‡,||}

[†]*Tyndall National Institute, Lee Maltings, Dyke Parade, Cork, Ireland*

[‡]*Department of Electrical and Electronic Engineering,
University College Cork, Cork, Ireland*

[§]*ilias.chlis@tyndall.ie*

[¶]*domenico.pepe@tyndall.ie*

^{||}*domenico.zito@tyndall.ie*

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Comparative Phase Noise analyses of common-source cross-coupled pair, Colpitts, Hartley and Armstrong differential oscillator circuit topologies, designed in 28 nm bulk CMOS technology in a set of common conditions for operating frequencies in the range from 1 GHz to 100 GHz, are carried out in order to identify their relative performance. The impulse sensitivity function (ISF) is used to carry out qualitative and quantitative analyses of the noise contributions exhibited by each circuit component in each topology, allowing an understanding of their impact on phase noise. The comparative analyses show the existence of five distinct frequency regions in which the four topologies rank unevenly in terms of best phase noise performance. Moreover, the results obtained from the ISF show the impact of flicker noise contribution as the major effect leading to phase noise degradation in nanoscale CMOS LC oscillators.

Keywords: Armstrong; CMOS; Colpitts; common-source cross-coupled differential pair; Hartley; nanoscale; oscillator topologies; phase noise; radiofrequency.

1. Introduction

Advances in wireless communications have a great impact on our societal and economic challenges.^{1–5} One of the most critical circuits of modern radiofrequency transceivers is the local oscillator, i.e., an autonomous circuit operating as the “pulsing heart” of such systems, in an analogy with the human body. As any other

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^{||}Corresponding author.

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solid-state circuits, oscillators are affected by the inherent noise of the electronic devices. One of the major negative effects of noise in oscillators is given by the induced variations on the instantaneous oscillation frequency, leading to the degradation of the spectral purity of the output voltage, referred as phase noise (PN).^{6,7} Oscillator PN performance directly affects the bit-error rate (BER) of the overall communication system.⁸

Understanding the generation mechanisms of PN has been a very intriguing challenge and consequently most of the efforts have been made in this direction for a number of circuit topologies.⁹ However, complete comparative studies have not been carried out on how to choose the oscillator circuit topology that could potentially offer the best performance in terms of PN for the range of operating frequencies of modern telecommunication systems. Usually, thanks to its reliable start-up, the common-source cross-coupled differential pair topology is chosen *a priori* without any further considerations. Thereby, from a designer perspective, such a comparative analysis could be very helpful in focusing the design efforts toward specific directions.

On the basis of the above motivations, in our recent works^{10,11} we dealt with this open question not addressed by the literature. In particular, we carried out a comparative analysis of PN of the common-source cross-coupled differential pair topology with Colpitts and Hartley single-ended topologies in 28 nm bulk CMOS technology for oscillation frequencies ranging from 1 GHz to 100 GHz. In that study, we made use of the impulse sensitivity function (ISF), $\Gamma(x)$,¹² which allowed us to quantify the noise contributions to the overall PN for each device in each oscillator circuit topology and identify the dominant noise sources and their impact versus the operating frequency.¹⁰ Interestingly, the results showed that there is not a superior topology in the absolute sense, but that the identification of the best circuit topology is related to the operating frequency range. In particular, the Hartley topology exhibited the best performance at higher frequency.¹⁰

Despite these results provide a first interesting perspective, this is limited by the comparison between a differential topology, i.e., cross-coupled common-source differential pair, and two single-ended topologies, Colpitts and Hartley. In fact, assuming a perfect symmetry, common-mode noise sources (e.g., noise coming from the common bias circuitry) do not produce effects in a differential topology; thereby, in principle, this aspect may play a significant role in determining the PN performance, then leading to a less effective comparison. Moreover, despite Colpitts and Hartley single-ended topologies have long been used in discrete circuit design, the advances in silicon integration have led to the implementation of differential versions as well,^{13,14} which have shown the potential for superior performance, typically at the expenses of larger area occupancy on silicon.

Consequently, extending the comparative analyses of PN carried out in Refs. 10 and 11 to the Colpitts and Hartley differential topologies is in order for a comparison under common conditions. Moreover, on the basis of the advances in integration and intrigued by the interesting results revealed by our previous analyses,^{10,11} it would be

useful in extending the study to other oscillator topologies which may deserve our attention, such as the Armstrong topology. A recent implementation of this circuit topology shows potential for very low power operation, while achieving a high spectral purity.¹⁵ This solution exploits integrated transformers^{16,17} in order to implement magnetic coupling between gate and drain terminals, as well as source and drain terminals of the transistor pair in the oscillator.

Driven by the above motivations, in this paper we report a comparative investigation of PN in the common-source cross-coupled pair, Colpitts, Hartley and Armstrong differential oscillator topologies, with the main objective of bringing to the light the contributions of the inherent noise sources in the most widespread oscillator topologies reported in the literature. This comparative analysis extends and complements the previous analysis,¹⁰ which was limited to Colpitts and Hartley single-ended topologies and common-source cross-coupled differential pair. Here, the comparative analysis is extended to differential topologies for a fair comparison with the common-source cross-coupled differential pair and extended also to the Armstrong topology (in addition to Colpitts and Hartley). The oscillator circuit topologies are investigated under the common design conditions, such as (a) power consumption, (b) supply voltage, (c) transistor current density and (d) sizing (area, aspect ratio, finger width), (e) inductance and (f) quality factor of the integrated spiral inductors, (g) coupling factor of the integrated transformers and (h) considering the full models of the transistors available within the process design kit, including all their parasitic components related to their actual size, but excluding the layout interconnections, since the additional parasitic components introduced by the layout implementation could mask the results of the topological investigations which are the objectives of our study. The common conditions adopted in this comparative analysis are the same as those adopted for the comparative analysis between Colpitts and Hartley single-ended topologies and common-source cross-coupled differential pair published in Ref. 10, thereby they represent the natural sequel from the previous results, which assures the continuity with them. As in the previous work,¹⁰ the ISF is used to quantify the impact of each noise source on the overall PN in each oscillator circuit topology, allowing the identification of the major contributions to the PN degradation versus the oscillation frequency. The results could drive the designer through the choice of the oscillator circuit topology that could potentially offer the best PN.

The paper is organized as follows. Section 2 describes the oscillator circuit topologies and their common design conditions. Section 3 reports the comparative analyses of PN. Section 4 reports the investigation on the contributions of each noise source to the overall PN. Finally, in Sec. 5 the conclusions are drawn.

2. Circuit Topologies

Figure 1 shows the oscillator circuit topologies designed in 28 nm bulk CMOS technology, operating from a 1 V supply voltage. All the circuit topologies operate in

Fig. 1. Schematic of the oscillator circuit topologies: (a) common-source cross-coupled differential pair; (b) differential Colpitts; (c) differential Hartley; (d) differential Armstrong. V_{B1} , V_{B2} , V_{B3} , V_{B4} , V_{B5} and V_{B6} are DC bias voltages.

the voltage-limited regime. The same figure shows the current impulsive sources acting parallel to the inherent current noise sources and used for the evaluation of the ISF. Based on the findings in Ref. 10, transient simulations were performed for an injected current amplitude of $1 \mu\text{A}$. The workload for the circuit simulations was significantly reduced by using OCEAN scripts.¹⁸

The sizes of the active and passive devices are reported in Table 1. Capacitors are considered ideal, whereas a quality factor (Q) of 10 is assumed for the spiral inductors, i.e., a feasible value for the oscillation frequencies in the range of interest from 1 GHz to 100 GHz.^{19,20} A coupling factor k of 0.85 is assumed for the transformers.¹³ For all the investigated differential circuit topologies the total power consumption is 6.3 mW, as in Ref. 10.

Table 1. Device sizing.

Osc. freq. (GHz)	Transistor width (μm)				Capacitor value (fF)				Inductor value (pH)
	M ₁	M ₂	M ₃	M ₄	C ₁	C ₂	C ₃	C ₄	L ₁
1	15	30	15	30	2500	5550	1410	5000	5000
10	15	30	15	30	229	527	132.5	469	500
100	15	30	15	30	5.7	29	4.72	15	50

In particular, the comparative analysis takes into account the common-source cross-coupled differential pair, Colpitts, Hartley and Armstrong differential circuit topologies shown in Figs. 1(a)–1(d), which have shown the best PN performances with respect to other design variations. Thereby, these topologies allow an effective comparison based on the actual needs and opportunities, rather than a comparison between basic topologies and their variations which are known from the literature to provide worse PN performance with respect to those considered in this comparative analysis. In other words, the investigated topologies are the most promising in their category. The common-source cross-coupled pair in Fig. 1(a) provides the negative resistance needed for the oscillation start-up. A p-MOSFET is chosen as a current source since it exhibits lower flicker noise. The transformer coupling in the Colpitts topology of Fig. 1(b) contributes to the suppression of common-mode oscillations.²¹ Moreover, for lower PN, two separate tail current transistors are used for biasing, as in Ref. 22. As for the Hartley topology in Fig. 1(c), the transformer coupling is used in order to reduce the area occupied by the inductors.²³ Finally, in the Armstrong topology of Fig. 1(d), the transformer coupling between gate and drain is considered for the same reasons. Also, in the latter topology, the inductance of the LC tank is given by the overall equivalent inductance offered by the self-inductance of the spiral inductors of the transformer and the mutual inductance between the two spirals on the gate and drain terminals of M₁.

3. Comparison of Phase Noise Performance

Figures 2–4 report the results in terms of PN obtained through the ISF and direct plots from periodic steady state (PSS) and periodic noise (Pnoise) simulations by SpectreRF in Cadence.

The ISF allows us to determine the flicker and thermal noise contributions to the overall PN, as reported in Figs. 2–4.¹¹ Consequently, the $1/f^3$ corner of the PN can be identified in each case. Table 2 provides the results for a 1 MHz frequency offset from the carrier. The results show that the PN predicted by ISF matches well (within 1.7 dB) with the values obtained directly by means of SpectreRF simulations.

From Table 2, it can be observed that under the adopted design conditions, common to all topologies, differential Armstrong topology reported here exhibits the lowest PN at an oscillation frequency of 1 GHz. The second best PN performance is

Fig. 2. PN versus frequency offset obtained through the ISF for a 1 μ A current impulse, and direct plot from PSS and Pnoise SpectreRF simulations, for the oscillation frequency of 1 GHz for: (a) common-source cross-coupled differential pair. The 1/f³ PN corner is at the frequency offset of 2 MHz; (b) differential Colpitts. The 1/f³ PN corner is at the frequency offset of 0.74 MHz; (c) differential Hartley. The 1/f³ PN corner is at the frequency offset of 3.7 MHz; (d) differential Armstrong. The 1/f³ PN corner is at the frequency offset of 0.34 MHz.

exhibited by the common-source cross-coupled topology, whereas Hartley follows closely and then Colpitts.

At the oscillation frequency of 10 GHz, the Armstrong topology considered in this study is superior in terms of PN performance to the other topologies under investigation. From the results obtained by SpectreRF, the cross-coupled and Hartley topologies are characterized by similar PN performance, whereas Colpitts shows the worst one.

Finally, at 100 GHz, the Hartley topology shows the best PN compared to the others. The Colpitts topology exhibits a PN higher than 10 dB with respect to Hartley. Then follows the common-source cross-coupled topology and last ranks Armstrong, which exhibit the worst PN.

Fig. 3. PN versus frequency offset obtained through the ISF for a 1 μ A current impulse and direct plot from PSS and Pnoise SpectreRF simulations, for the oscillation frequency of 10 GHz for: (a) common-source cross-coupled differential pair. The 1/f³ PN corner is at the frequency offset of 7.5 MHz; (b) differential Colpitts. The 1/f³ PN corner is at the frequency offset of 8 MHz; (c) differential Hartley. The 1/f³ PN corner is at the frequency offset of 10 MHz; (d) differential Armstrong. The 1/f³ PN corner is at the frequency offset of 2.1 MHz.

In order to gain a better understanding of the performances in between the initial discrete set of frequencies, the topologies have been designed also for the additional operating frequencies of 30, 50 and 70 GHz. The PN at a 1 MHz offset from the carrier frequency obtained by direct plots from PSS and Pnoise simulations is shown in Fig. 5. By inspection, Fig. 5 reveals five distinct regions in which the topologies rank unevenly in terms of best PN performance.

Region 1 (1–10 GHz): The Armstrong topology exhibits the lowest PN, whereas the Colpitts topology exhibits the worst one. In between, the common-source cross-coupled topology shows PN performance very close to that given by the Hartley topology.

Fig. 4. PN versus frequency offset obtained through the ISF for a $1\mu\text{A}$ current impulse and direct plot from PSS and Pnoise SpectreRF simulations, for the oscillation frequency of 100 GHz for: (a) common-source cross-coupled differential pair. The $1/f^3$ PN corner is at the frequency offset of 5.5 MHz; (b) differential Colpitts. The $1/f^3$ PN corner is at the frequency offset of 20 MHz; (c) differential Hartley. The $1/f^3$ PN corner is at the frequency offset of 7.4 MHz; (d) differential Armstrong. The $1/f^3$ PN corner is at the frequency offset of 14 MHz.

Table 2. Summary of PN performance.

Topology	PN [dBc/Hz] @ 1 MHz frequency offset					
	1 GHz		10 GHz		100 GHz	
	SpectreRF	ISF	SpectreRF	ISF	SpectreRF	ISF
Cross-coupled	-123.7	-124.06	-102.66	-102.69	-74.78	-75.79
Colpitts	-118.34	-119.71	-99.56	-100.26	-78.45	-78.27
Hartley	-121.69	-123.38	-102.59	-104.15	-89.78	-89.00
Armstrong	-127.51	-128.22	-106.12	-106.57	-72.34	-73.74

Fig. 5. PN at a 1 MHz frequency offset from the carrier frequency obtained by direct plots from PSS and Pnoise simulations, versus oscillation frequency for the common-source cross-coupled differential pair, as well as for the differential Colpitts, Hartley and Armstrong oscillator circuit topologies.

Region 2 (10–20 GHz): The Armstrong still exhibits the best PN and Colpitts the worst one. On the other hand, Hartley gradually improves with respect to the other topologies. On an average, the common-source cross-coupled pair is characterized by a PN 2.5 dB lower than Colpitts.

Region 3 (20–40 GHz): The Hartley topology exhibits the lowest PN. The comparison with the others improves as the oscillation frequency increases. Here, Armstrong exhibits the second best PN performance, whereas the Colpitts topology still exhibits the worst one. On an average, the common-source cross-coupled pair shows a PN 1.2 dB lower than Colpitts.

Region 4 (40–70 GHz): The differential Armstrong topology shows the worst performance, and the cross-coupled and Colpitts do not show better performance. The Hartley topology keeps increasing its superior performance with respect to the others. In particular, at 70 GHz, the differential Hartley topology shows a PN of about 10 dB lower with respect to the others.

Region 5 (70–100 GHz): The differential Hartley is still characterized by the best PN, whereas Armstrong continues to exhibit the most degraded output signal spectrum. Here the Colpitts topology exhibits a better PN with respect to the common-source cross-coupled topology. In particular, their PN is on an average 3.5 and 2 dB, respectively, lower than differential Armstrong.

Thereby, it can be concluded that for oscillation frequencies between 1 and 20 GHz, the Armstrong oscillator circuit topology considered here could be potentially the best choice. Outside this range, between 20 and 100 GHz, its performance dramatically deteriorates. For this oscillation frequency range, the differential

Hartley topology considered in this study appears to be potentially the best choice. It is worth observing that the superior PN performance of the differential Hartley topology at high frequencies confirms with the results emerged from Ref. 10 for the single-ended Hartley topology.

4. Contributions of the Device Noise to Phase Noise

In order to get insight into the above results, in this section we report the evaluations of the contributions from each noise source in each oscillator circuit topology for a discrete set of oscillation frequencies from 1 GHz to 100 GHz, carried out by means of the ISF. The total thermal noise contribution to the PN, the latter traditionally indicated with $\mathcal{L}$, from all m noise sources with a white power spectral density, can be expressed as¹²:

$$\mathcal{L}\{\Delta\omega\}_{\text{white}} = \sum_{i=1}^m \left[\left(\frac{\Gamma_{\text{rms}}^2}{q_{\text{max}}^2} \right)_i \frac{\left(\frac{\bar{i}_n^2}{\Delta f} \right)_i}{2\Delta\omega^2} \right], \quad (1)$$

where $\left(\frac{\bar{i}_n^2}{\Delta f} \right)_i$ is the thermal noise generated from the i th noise source, q_{max} is the charge injected into a circuit node by the noise source i_n insisting in that node, Γ_{rms} is the root mean square (rms) value of the ISF and $\Delta\omega$ is the offset from the oscillation angular frequency. The contribution of each noise source with white spectrum to the total thermal noise appearing at the output spectrum of the oscillator, the latter given by (1), is independent of the angular frequency offset $\Delta\omega$ as seen from (2).

$$\frac{[\mathcal{L}\{\Delta\omega\}_{\text{white}}]_i}{\mathcal{L}\{\Delta\omega\}_{\text{white}}} = \frac{\left(\frac{\Gamma_{\text{rms}}^2}{q_{\text{max}}^2} \right)_i \left(\frac{\bar{i}_n^2}{\Delta f} \right)_i}{\sum_{i=1}^m \left[\left(\frac{\Gamma_{\text{rms}}^2}{q_{\text{max}}^2} \right)_i \left(\frac{\bar{i}_n^2}{\Delta f} \right)_i \right]}. \quad (2)$$

Moreover, the total flicker contribution to the PN, from all n noise sources with a $1/f$ (flicker) spectrum can be expressed as follows¹²:

$$\mathcal{L}\{\Delta\omega\}_{1/f} = \sum_{i=1}^n \left[\left(\frac{4\Gamma_{\text{DC}}^2}{q_{\text{max}}^2} \right)_i \frac{\left(\frac{\bar{i}_n^2}{\Delta f} \right)_i}{8\Delta\omega^2} \frac{(\omega_{1/f})_i}{\Delta\omega} \right], \quad (3)$$

where $\left(\frac{\bar{i}_n^2}{\Delta f} \right)_i \times \frac{(\omega_{1/f})_i}{\Delta\omega}$ is the flicker noise generated from the i th noise source, Γ_{DC} is the DC value of the ISF and $(\omega_{1/f})_i$ is the flicker noise corner of the i th active device. From (3) it can be concluded that larger oscillation amplitude leads to lower flicker noise contribution to PN, since $q_{\text{max}} = C \times V_{\text{max}}$, where C is the total tank capacitance and V_{max} is the maximum voltage swing across the tank.¹² The contribution of

each flicker noise source to the total flicker noise appearing at the output spectrum of the oscillator, the latter given by (3), is independent from the angular frequency offset $\Delta\omega$ as noted from (4).

$$\frac{[\mathcal{Z}\{\Delta\omega\}]_{1/f}}{\mathcal{Z}\{\Delta\omega\}} = \frac{\left(\frac{\Gamma_{DC}^2}{q_{max}^2}\right)_i \left(\frac{\overline{i_n^2}}{\Delta f}\right)_i (\omega_{1/f})_i}{\sum_{i=1}^n \left[\left(\frac{\Gamma_{DC}^2}{q_{max}^2}\right)_i \left(\frac{\overline{i_n^2}}{\Delta f}\right)_i (\omega_{1/f})_i\right]}. \quad (4)$$

Figures 6–8 report the percent contributions of the active and passive device noise sources to the flicker and thermal noise components of the PN. They also show the

Fig. 6. Relative flicker noise contributions to PN from active devices in the oscillator circuit topologies for: (a) common-source cross-coupled differential pair; (b) differential Colpitts; (c) differential Hartley; (d) differential Armstrong. The contribution of each noise source to the flicker noise appearing at the output spectrum of the oscillator, is independent of the angular frequency offset $\Delta\omega$ as seen from (4).

Fig. 7. Relative thermal noise contributions to PN from active and passive devices in the oscillator circuit topologies for: (a) common-source cross-coupled differential pair; (b) differential Colpitts; (c) differential Hartley; (d) differential Armstrong. The contribution of each noise source to the thermal noise appearing at the output spectrum of the oscillator, is independent of the angular frequency offset $\Delta\omega$ as seen from (2).

total contributions of each device to PN at a frequency offset of 1 MHz from the oscillation frequency. These results allow us to derive several important observations.

For the 1 GHz oscillation frequency, in the common-source cross-coupled pair topology, the flicker noise sources of the cross-coupled pair contribute for about 65% to the flicker noise component of the PN, as shown in Fig. 6(a). From Fig. 7(a), it can be observed that only 13% of the thermal noise component of PN comes from the thermal noise of the cross-coupled pair. In spite of all, Fig. 8(a) shows that the total noise from the cross-coupled pair is the major contribution to the PN at a 1 MHz frequency offset. This can be explained by noticing from Fig. 2(a) that the $1/f^3$ corner of the PN is at the frequency offset of 2 MHz.

Fig. 8. Relative total noise contributions to PN, from active and passive devices in the oscillator circuit topologies at a 1 MHz offset from the carrier frequency for: (a) common-source cross-coupled differential pair; (b) differential Colpitts; (c) differential Hartley; (d) differential Armstrong.

In the Colpitts topology, from Figs. 6(b) and 7(b) both the flicker noise and thermal noise components of the PN are mainly due to the tail current transistor pair M_3 . This explains why at a 1 MHz frequency offset, the tail current transistor pair M_3 takes the largest portion of the total PN as reported in Fig. 8(b). With respect to the differential Hartley, the active device pair M_1 is the only source of flicker noise. In addition, the thermal noise generated by M_1 pair is mainly responsible for the white noise affecting the PN. This is why at a 1 MHz frequency offset, the total noise contribution to PN is dominated by the M_1 common-source cross-coupled pair.

Last, from Figs. 6(d) and 7(d) M_1 transistor pair in the Armstrong topology is responsible for about 65% and 60% of the PN components due to flicker noise and thermal noise, respectively. Thereby, it is also responsible for most of the total PN (62%) as shown in Fig. 8(d).

For the oscillation frequency of 10 GHz, in the common-source cross-coupled pair topology, from Fig. 6(a) the cross-coupled pair M_1 is the major contributor to the flicker noise component of PN. Also, at a 1 MHz offset the PN spectrum is still at the $1/f^3$ region according to Fig. 3(a). Thereby, the cross-coupled pair M_1 is expected to be the dominant source of the overall PN as confirmed from Fig. 8(a).

As for the Colpitts topology, the flicker contribution of the tail current transistor pair M_3 is predominant. Thereby, for the same reason as above, the tail current noise is the major contributor to PN at a 1 MHz frequency offset.

The pair of transistors M_1 in differential Hartley is almost the sole source of noise. This is because the noise generated by the parasitic resistance of the inductors is at least one order of magnitude lower than the flicker and thermal noise of the active device pair M_1 .

Finally, the tail current transistor M_4 in the Armstrong topology is mostly responsible for the flicker component of PN. Moreover, the $1/f^3$ PN corner is at 2.1 MHz, as depicted in Fig. 3(d). Therefore, at a 1 MHz offset the tail current transistor M_4 presents the main contribution to the overall PN.

For the oscillation frequency of 100 GHz, the $1/f^3$ frequency corners of PN in the four topologies under investigation are beyond 5 MHz, according to Figs. 4(a)–4(d). Consequently, at a 1 MHz frequency offset the PN is mostly due to the flicker noise. In particular, in the common-source cross-coupled topology, the cross-coupled pair M_1 and the p-MOSFET current source M_2 show similar contributions to the flicker noise component of PN and to the overall PN. This happens in spite of the higher thermal noise component of PN from the tail current transistor M_2 .

In the Colpitts topology, flicker and thermal noise contributions to PN are mainly due to M_1 transistor pair. Thereby, the pair of transistors M_1 represents the noise source which is mainly responsible for the PN at a 1 MHz frequency offset.

In the Hartley topology, the active device pair M_1 is the only flicker noise source, which dominates the PN at a 1 MHz frequency offset.

In the Armstrong topology, almost equal contribution to the flicker and thermal noise components of PN from the M_1 transistor pair and the tail current transistor M_4 , also means equal contribution to the overall PN at a 1 MHz frequency offset.

From all the above, we can conclude that, for all four topologies and for the oscillation frequencies of 10 and 100 GHz, the $1/f^3$ region of the PN extends above 1 MHz. At an oscillation frequency of 1 GHz, this is true for the common-source cross-coupled pair and for the Hartley topologies. This is a consequence of the adoption of nanoscale CMOS technologies characterized by flicker noise corners of several tens or hundreds of MHz, which lead to flicker noise up-conversion being responsible for most of PN^{24,25} even at large offsets from the carrier frequency. This means that the devices with the highest contribution to the flicker noise presented at the output spectrum will also dominate PN. Hence, design efforts should be made in minimizing the flicker noise sources as much as possible, as well as flicker noise up-conversion

characteristic mechanisms in each topology. For example, increasing the width of the cross-coupled devices of Fig. 1(a) would reduce the flicker noise produced by the transistor pair M_1 . On the other hand, flicker noise up-conversion gain would be increased. This is due to the increased small-signal loop gain which would in turn cause a higher distortion of the voltage output.^{25,26} As another example, a filtering technique adopting a resonant filter could also be adopted for reducing flicker noise up-conversion.²⁷

For the oscillation frequency of 1 GHz, in the Colpitts and Armstrong topologies the $1/f^3$ PN corners are below the 1 MHz frequency offset. In this case, the active or passive devices with the highest contribution to the thermal noise component of the PN will be dominant. Short channel effects such as velocity saturation and channel length modulation are responsible for the significant increase in the thermal noise excess factor γ in deep submicron CMOS technologies.^{28,29} Thus, thermal noise from the active devices is usually the principal source of white noise in the output spectrum as already observed from Figs. 6–8.

The theoretical expressions of the overall PN including all its contributions that could allow us to distinguish between the nature of the flicker noise contributions due to the up-conversion mechanisms identified in the literature²⁵ could be addressed in future works. Theoretical analysis of flicker noise up-conversion is outside the scope of this manuscript, for which we refer to the existing literature.^{25,30,31} However, it is worth observing that due to the absence of varactor, flicker noise up-conversion is caused mainly by (a) amplitude to PN conversion due to nonlinear transconductor parasitic capacitance, as well as by (b) modulation of the harmonic content of the output voltage waveform, i.e., Groszkowski effect.²⁵ Reference 30 reports an analysis which is based on the ideal quadratic I-V MOS characteristic, and, as such, quantitatively valid only for long-channel transistors. Thereby, the conclusion reported therein³⁰ that there is no up-conversion of $1/f$ noise into PN from the core MOS transistors (M_1) does not apply to the oscillator circuit topologies investigated in this manuscript since they adopt short channel MOSFETs of the 28 nm bulk CMOS technology.

5. Conclusions

Comparative analyses of phase noise were carried out for four differential oscillator circuit topologies: common-source cross-coupled pair, Colpitts, Hartley and Armstrong. The oscillator circuit topologies were designed in a 28 nm bulk CMOS technology, for a set of operating frequencies in the range from 1 GHz to 100 GHz. All the topologies were investigated under the same common design conditions, such as power consumption, supply voltage, transistor current density and sizing, inductance and quality factor of the integrated spiral inductors, coupling factor of the integrated transformers, and considering the full models of the transistors available within the process design kit, including all their parasitic components related to their actual

size. Furthermore, the phase noise results from PSS and Pnoise simulations were compared with phase noise predictions obtained by the ISF. Finally, the noise contributions from each active or passive device in the circuit topologies to the flicker and thermal phase noise components and to the overall phase noise at a 1 MHz frequency offset from carrier frequency were evaluated and discussed.

The results show that, under the adopted design conditions, the phase noise of the four topologies degrades unevenly over the considered oscillation frequency range. In particular, the comparative analyses show the existence of five distinct frequency regions. Thereby, the results presented here suggest that the identification of the best oscillator circuit topology in terms of phase noise is related to the operating frequency range. Consequently, these results suggest the opportunity to address further investigations on the Armstrong and Hartley topologies considered in this study. The investigations could allow us to extend the range of possibilities beyond the common practice of choosing the common-source cross-coupled differential pair topology, traditionally selected for its reliable start-up, but without further topological considerations.

Finally, the investigations through the ISF allowed the identification of the dominant noise contributions for each oscillator circuit topology. Despite a few exceptions, the results showed that the flicker noise from the active devices is the component with the most significant effect on the oscillator phase noise at a 1 MHz frequency offset from the carrier frequency, confirming the rising role of flicker noise in nanoscale CMOS technology.

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