The effect of the thickness of tunneling layer on the memory properties of $(\text{Cu}_2\text{O})_{0.5}(\text{Al}_2\text{O}_3)_{0.5}$ high- k composite charge-trapping memory devices

Jinqiu Liu, Jianxin Lu, Jiang Yin*, Bo Xu, Yidong Xia and Zhiguo Liu

*National Laboratory of Solid State Microstructures,
College of Engineering and Applied Sciences,
Nanjing University, Nanjing, Jiangsu 210093, China
jyin@nju.edu.cn

Received 20 March 2016

Revised 10 May 2016

Accepted 12 May 2016

Published 1 June 2016

The charge-trapping memory devices namely $\text{Pt}/\text{Al}_2\text{O}_3/(\text{Al}_2\text{O}_3)_{0.5}(\text{Cu}_2\text{O})_{0.5}/\text{SiO}_2/p\text{-Si}$ with 2, 3 and 4 nm SiO_2 tunneling layers were fabricated by using RF magnetron sputtering and atomic layer deposition techniques. At an applied voltage of ± 11 V, the memory windows in the C - V curves of the memory devices with 2, 3 and 4 nm SiO_2 tunneling layers were about 4.18, 9.91 and 11.33 V, respectively. The anomaly in memory properties among the three memory devices was ascribed to the different back tunneling probabilities of trapped electrons in the charge-trapping dielectric $(\text{Al}_2\text{O}_3)_{0.5}(\text{Cu}_2\text{O})_{0.5}$ due to the different thicknesses of SiO_2 tunneling layer.

Keywords: Memory device; tunneling layer; charge-trapping; composite.

1. Introduction

Silicon-oxide-nitride-oxide-silicon (SONOS)-type memory devices as one of the non-volatile flash memories have found wide applications, such as in cell phones, computers and communication,^{1–7} in which the charges are stored in the nitride layer, not compatible with dimensional scaling, leading to poor performance in program/erase (P/E) speed and retention.^{8–20} To achieve good memory characteristics, some high- k oxide dielectrics have been proposed and studied as the tunneling layer, charge-trapping layer and blocking layer, respectively. For example, HfO_2 , ZrO_2 , Y_2O_3 and La_2O_3 have been employed to replace Si_3N_4 in SONOS memory devices to acquire better trapping characteristics,^{21–23} and Al_2O_3 has been employed as the tunneling

*Corresponding author.

This is an Open Access article published by World Scientific Publishing Company. It is distributed under the terms of the Creative Commons Attribution 4.0 (CC-BY) License. Further distribution of this work is permitted, provided the original work is properly cited.

layer and the blocking layer to reduce the working voltage.²⁴ For a charge-trapping memory (CTM) device, the charge-trapping layer with a high charge-trapping capability in a small scale is critically important for further applications in the future.

New structures derived from SONOS-type memory device have been proposed to improve the charge-trapping ability and reliability, such as the multilayered charge-trapping memory devices, including $\text{HfO}_2/\text{ZrO}_2/\text{HfO}_2$, $\text{HfO}_2/\text{Al}_2\text{O}_3/\text{HfO}_2$, etc., which show wonderful charge storage and retention properties as compared with those memory devices with single charge-trapping layer.^{25–30} Some definite experimental evidences identified that the charge-trapping behaviors in these multilayered memory devices should be ascribed to the inter-diffusion at the interface of different high- k oxides.^{25–28}

Recently, some high- k composite oxides have been employed as the charge-trapping dielectrics to achieve a higher density of trapped charges in CTM devices.^{31–33} It was reported that the memory structure with a charge-trapping layer of $(\text{Al}_2\text{O}_3)_{0.5}(\text{Cu}_2\text{O})_{0.5}$ (named as CAO) shows a large memory window and a high density of the trapped charges.³⁴

In this paper, we report the effect of the thickness of tunneling layer on the memory properties of $(\text{Al}_2\text{O}_3)_{0.5}(\text{Cu}_2\text{O})_{0.5}$ CTM device.

2. Experimental

P-type (100) Si wafers with a resistivity of $1\text{--}10\ \Omega\cdot\text{cm}$ were cleaned by the standard Radio Corporation of America (RCA) process. Then the native oxide layer was removed by dipping the wafer in dilute HF solution for 2 min. SiO_2 layers with thicknesses of 2, 3 and 4 nm were grown on *P*-type (100) Si wafer by using a traditional thermal oxidation process, respectively. Three kinds of $\text{Al}_2\text{O}_3\text{--Cu}_2\text{O}$ CTM devices with different thicknesses of SiO_2 tunneling layer were fabricated, as schematically drawn in Fig. 1. The thin films $(\text{Al}_2\text{O}_3)_{0.5}(\text{Cu}_2\text{O})_{0.5}$ were deposited as the charge-trapping layers for the three CAO CTM devices by using RF magnetron sputtering technique with a mixed ceramic target. The CAO target was prepared

Fig. 1. The schematic drawing of three CAO CTM devices with (a) 2 nm, (b) 3 nm and (c) 4 nm SiO_2 tunneling layers.

by sintering a cold-pressed $\text{Al}_2\text{O}_3\text{--Cu}_2\text{O}$ powder pellet at 1500°C for 6 h. Before pressing and sintering, the mixed powder of $\text{Al}_2\text{O}_3\text{--Cu}_2\text{O}$ was ball milled for 20 h. The chamber for RF sputtering was under a mixed ambience of argon and oxygen (3:1) at 4 Pa, and RF power was 100 W. The silicon wafer covered with SiO_2 and CAO layers was transferred to the atomic layer deposition (ALD) reactor chamber, and Al_2O_3 film with a thickness of 14 nm was deposited as the blocking layer at 200°C with $\text{Al}(\text{CH}_3)_3$ as the precursor. Before depositing the top electrode Pt on Al_2O_3 blocking layer, the memory devices had underwent a rapid annealing treatment (RTA) at 200°C in N_2 for 40 s.

Keithley 4200 semiconductor characterization system (Keithley 4200 SCS) was used to characterize the memory properties of the CAO memory devices at CasCade Summit 12000B-M platform. The cross-sectional morphology of those devices was characterized by using a high-resolution transmission electron microscopy (HRTEM) (Tecnai F20).

3. Results and Discussion

The cross-sectional HRTEM images of three CAO CTM devices are shown in Figs. 2(a)–2(c), respectively. It was observed that the interface between Si and SiO_2 is quite sharp. The thicknesses of the SiO_2 tunneling layer in the three CTM devices are about 2, 3 and 4 nm, respectively. The tunneling layer of SiO_2 and the blocking layer of Al_2O_3 all show an amorphous structure.

The capacitance–voltage ($C\text{--}V$) characteristics of CAO memory devices at 1 MHz are shown in Figs. 3(a)–3(c), respectively. The $C\text{--}V$ curves were first measured by sweeping the gate voltage from $+7\text{ V}$ to -7 V and then back to $+7\text{ V}$ at a rate of 0.5 V/s , in a step of 0.1 V . The memory windows, defined as the difference of the flat-band voltages (V_{fb}) between the program and erase states, were 1.73, 3.48 and 5.44 V for CAO CTM devices with the 2, 3 and 4 nm SiO_2 tunneling layers at the applied gate voltages of $\pm 7\text{ V}$, respectively.

Fig. 2. The cross-sectional HRTEM images of the three CAO CTM devices with (a) 2 nm, (b) 3 nm and (c) 4 nm SiO_2 tunneling layers.

Fig. 3. The capacitance–voltage (C – V) characteristics of CAO memory devices with (a) 2 nm, (b) 3 nm and (c) 4 nm SiO_2 tunneling layers at 1 MHz.

During the program process for CAO CTM devices, the state of the charge carriers in Si channel will undergo a series of transitions: accumulation $\rightarrow$ depletion $\rightarrow$ inversion. At an applied positive gate voltage larger than the flat-band voltage, the positive electric field will be formed between the gate electrode (Pt) and Si channel. At a strong positive electric field, charge carriers in the surface region of Si channel will be in a state of inversion, and electrons are the main charge carriers. The positive electric field will force electrons in the surface of Si channel to move across the tunneling layer, and then they get trapped in CAO charge-trapping layer. The equivalent capacitance circuits corresponding to three CAO CTM devices were also shown in Figs. 1(a), 1(b) and 1(c), respectively, where C_0 is the capacitance of the structure including CAO layer and Al_2O_3 layer; and C_1 , C_2 and C_3 represent the capacitances of SiO_2 layer with different thicknesses. At a definite applied voltage V , the electric fields across the tunneling layers of SiO_2 in the three CAO memory devices can be written as:

$$E_1 = \frac{V}{\frac{\varepsilon S}{C_0} + d_1}, \quad (1)$$

$$E_2 = \frac{V}{\frac{\varepsilon S}{C_0} + d_2} = \frac{V}{\frac{\varepsilon S}{C_0} + 1.5d_1}, \quad (2)$$

$$E_3 = \frac{V}{\frac{\varepsilon S}{C_0} + d_3} = \frac{V}{\frac{\varepsilon S}{C_0} + 2d_1}. \quad (3)$$

Here, ε represents dielectric constant of SiO_2 , S represents the area of the electrode and d_1 , d_2 and d_3 represent the thicknesses of SiO_2 layers in the three CAO CTM devices. It means that the CAO CTM device (d_3) with a 4 nm SiO_2 layer will lead to the lowest electric field across the tunneling layer under an applied voltage V , and that the CAO CTM device (d_1) with a 2 nm SiO_2 layer will lead to the largest electric field across the tunneling layer. Thus, a largest memory window should be expected in d_1 , just as observed in HfO_2 charge-trapping memory devices.^{35,36}

In contrast, a lowest memory window was obtained in the C - V curve of d_1 , and a largest memory window was obtained for d_3 with the 4 nm SiO_2 layer. The anomalies in the C - V curves of CAO CTM devices may be related to the inter-diffusion of Cu at the interface SiO_2/CAO , although it was not observed from HRTEM images of the three CAO CTM devices due to the limitation of HRTEM resolution. After the removal of applied electric field, some electrons trapped inside SiO_2 tunneling layer may directly tunnel back to Si substrate due to the ultrathin tunneling layer. In addition, the inter-diffusion of Cu at the interface SiO_2/CAO also reduces the density of defect states in CAO charge-trapping memory devices due to the reduction of Cu_2O composition. Due to the thicker tunneling layers in d_2 and d_3 , the effect of the inter-diffusion of Cu at the interface SiO_2/CAO on the memory window may decrease, so little difference in the memory windows between two devices was observed. On the other hand, the different back tunneling effects of trapped electrons from CAO charge-trapping layer to Si channel also may be responsible for the anomalies in the C - V curves of CAO CTM devices. After the removal of applied electric field, the thinner layer of SiO_2 leads to the larger back tunneling probability of the trapped electrons.

From Fig. 3, with the increase of sweeping voltage, the memory window in the C - V curve of CAO CTM devices did increased quickly. At the sweeping gate voltages of ± 11 V, the memory window in the C - V curves of d_1 with 2 nm SiO_2 tunneling layer was obtained as 4.18 V. For d_2 with a 3 nm SiO_2 tunneling layer, about 1.5 times in thickness to that in d_1 , the memory window was significantly increased as 9.91 V. A little increase in its memory window as 11.33 V was observed in d_3 with a 4 nm SiO_2 tunneling layer, 2 times in thickness to that in d_1 . It means the optimized thickness of SiO_2 tunneling layer for CAO memory devices should be around 4 nm. The density of the trapped charges per unit area (N_t) can be estimated by using Eq. (4):

$$N_t = \frac{C_{ox}\Delta V_{fb}}{qA}, \quad (4)$$

where C_{ox} is the capacitance of the memory device in the accumulation region; q is the electron charge; and A represents the effective area of Pt electrode, in this case $A = 1.77 \times 10^{-4} \text{ cm}^2$. The densities of trapped charges in CAO CTM devices with 2, 3 and 4 nm SiO_2 tunneling layers at the applied voltages of ± 11 V were calculated as $7.27 \times 10^{12} \text{ cm}^{-2}$, $1.46 \times 10^{13} \text{ cm}^{-2}$ and $1.62 \times 10^{13} \text{ cm}^{-2}$, respectively.

Figure 4 shows the P/E characteristics of three CAO CTM devices. Pulses of +10 V, 10 ms and -10 V, 10 ms were applied to evaluate the characteristics of the P/E operations. d_3 with a 4 nm SiO_2 tunneling layer shows a better performance as compared with d_1 and d_2 , in accordance with the characteristics of their C - V curves. It can also be observed that for the three CAO CTM devices, the erase speeds are larger than the program speeds.

The retention properties of the three CAO CTM devices were shown in Fig. 5. d_1 with a 2 nm SiO_2 tunneling layer shows the largest decrease in its V_{fb} -shift

Fig. 4. The program/erase (P/E) characteristics of three CAO CTM devices.

Fig. 5. The retention characteristics of three CAO CTM devices.

due to the largest back tunneling probability of the trapped electrons in CAO charge-trapping layer, and d_3 with a 4 nm SiO_2 tunneling layer shows the best retention property due to its thick tunneling layer. From Fig. 5, the trend of charge loss transient was the same for the three CAO memory devices, different with the one that was reported in HfO_2 charge-trapping memory devices.³⁵ It also may be related to the inter-diffusion of Cu at the interface SiO_2/CAO , although further investigation is needed.

4. Conclusion

In summary, the CTM devices with a structure $\text{Pt}/\text{Al}_2\text{O}_3/(\text{Cu}_2\text{O})_{0.5}(\text{Al}_2\text{O}_3)_{0.5}/\text{SiO}_2/p\text{-Si}$ have been fabricated. At a definite applied voltage, the memory device with a 2 nm SiO_2 tunneling layer has the lowest memory window in its C - V curve, and the memory device with a 4 nm SiO_2 tunneling layer has the largest memory window in its C - V curve. It was proposed that the differences in

charge-trapping abilities of the three $(\text{Cu}_2\text{O})_{0.5}(\text{Al}_2\text{O}_3)_{0.5}$ charge-trapping memory devices should be attributed to the different back tunneling probabilities of trapped electrons due to the different thicknesses of SiO_2 tunneling layers. By optimizing the thicknesses of the tunneling layer, $(\text{Cu}_2\text{O})_{0.5}(\text{Al}_2\text{O}_3)_{0.5}$ charge-trapping memory devices may show some potential to respond to the challenge of further scaling down for the non-volatile memory devices in the future.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (Grant Nos. 61176124 and 11204123).

References

1. P. Chakraborty, S. S. Mahato, T. K. Maiti, M. K. Bera, C. Mahata, S. K. Samanta, A. Biswas and C. K. Maiti, *Microelectron. Eng.* **86** (2009) 299.
2. T. Baron, B. Pellissier, L. Perniola, F. Mazen, J. M. Hartmann and G. Polland, *Appl. Phys. Lett.* **83** (2003) 1444.
3. G. W. Burr, B. N. Kurdi, J. C. Scott, C. H. Lam, K. Gopalakrishnan and R. S. Shenoy, *IBM J. Res. Dev.* **52** (2008) 449.
4. V. V. Afanas'ev, M. Houssa, A. Stesmans, C. Merckling, T. Schram and J. A. Kittl, *Appl. Phys. Lett.* **99** (2011) 072103.
5. M. Burkhardt, A. Jedaa, M. Novak, A. Ebel, K. Voitchovsky, F. Stellacci, A. Hirsch and M. Halik, *Adv. Mater.* **22** (2010) 2525.
6. S. Haddad, C. Chang, B. Swaminathan and J. Lien, *IEEE Electron Device Lett.* **10** (1989) 117.
7. J. K. Bu and M. H. White, *Solid State Electron.* **45** (2001) 47.
8. S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe and K. Chan, *Appl. Phys. Lett.* **68** (1996) 1377.
9. H. I. Hanafi, S. Tiwari and I. Khan, *IEEE Trans. Electron Devices* **43** (1996) 1553.
10. D. Kim, D. U. Lee, E. K. Kim and W. J. Cho, *Appl. Phys. Lett.* **101** (2012) 233510.
11. R. C. Jeff Jr., M. Yun, B. Ramalingam, B. Lee, V. Misra, G. Triplett and S. Gangopadhyay, *Appl. Phys. Lett.* **99** (2011) 072104.
12. S. Kundu, N. N. Halder, P. Biswas, D. Biswas, P. Banerji, R. Mukherjee and S. Chakraborty, *Appl. Phys. Lett.* **101** (2012) 212108.
13. T. K. Kang, H. W. Liu, F. H. Wang, C. L. Lin, T. C. Liao and W. F. Wu, *Solid State Electron.* **61** (2011) 100.
14. J. H. Kim, J. Y. Yang, J. S. Lee and J. P. Hong, *Appl. Phys. Lett.* **92** (2008) 013512.
15. F. M. Yang, T. C. Chang, P. T. Liu, U. S. Chen, P. H. Yeh, Y. C. Yu, J. Y. Lin, S. M. Sze and J. C. Lou, *Appl. Phys. Lett.* **90** (2007) 222104.
16. J. H. Chen, W. J. Yoo, D. S. H. Chan and L. J. Tang, *Appl. Phys. Lett.* **86** (2005) 073114.
17. C. Bonafos, M. Carrada, G. Benassayag, S. S. Chardon, J. Groenen, V. Paillard, B. Pecassou, A. Claverie, P. Dimitrakakis, E. Kapetanakis, V. I. Sougleridis, P. Normand, B. Sahu and A. Slaoui, *Mater. Sci. Semicond. Process.* **15** (2012) 615.
18. T. Z. Lu, M. Alexe, R. Scholz, V. Talalaev, R. J. Zhang and M. Zacharias, *J. Appl. Phys.* **100** (2006) 014310.
19. Q. Wan, C. L. Lin, W. L. Liu and T. H. Wang, *Appl. Phys. Lett.* **82** (2003) 4708.

20. Y. Zhou, J. Yin, H. N. Xu, Y. D. Xia, Z. G. Liu, A. D. Li, Y. P. Gong, L. Pu, F. Yan and Y. Shi, *Appl. Phys. Lett.* **97** (2010) 143504.
21. H. C. You, T. H. Hsu, F. H. Ko, J. W. Huang, W. L. Yang and T. F. Lei, *IEEE Electron Device Lett.* **27** (2006) 653.
22. T. H. Tsu, H. C. You, F. H. Ko and T. F. Lei, *J. Electrochem. Soc.* **153** (2006) 934.
23. Y. H. Lin, C. H. Chien, T. Y. Yang and T. F. Lei, *J. Electrochem. Soc.* **154** (2007) 619.
24. C. Lee, S. Hur, Y. Shin, J. Choi, D. Park and K. Kim, *Appl. Phys. Lett.* **86** (2005) 152908.
25. Z. Tang, X. Zhu, H. Xu, Y. Xia, J. Yin, Z. Liu, A. D. Li and F. Yan, *Mater. Lett.* **92** (2013) 21.
26. X. X. Lan, X. Ou, Y. Q. Cao, S. Y. Tang, C. J. Gong, B. Xu, Y. D. Xia, J. Yin, A. D. Li, F. Yan and Z. G. Liu, *J. Appl. Phys.* **114** (2013) 044104.
27. X. X. Lan, X. Ou, Y. Lei, C. J. Gong, Q. N. Yin, B. Xu, Y. D. Xia, J. Yin and Z. G. Liu, *Appl. Phys. Lett.* **103** (2013) 192905.
28. Y. Shi, K. Saito, H. Ishikuro and T. Hiramoto, *J. Appl. Phys.* **84** (1998) 2358.
29. M. Yang, T. P. Chen, Z. Liu, J. I. Wong, W. L. Zhang, S. Zhang and Y. Liu, *J. Appl. Phys.* **106** (2009) 103701.
30. C. H. Lin and Y. Kuo, *J. Appl. Phys.* **110** (2011) 024101.
31. C. J. Gong, Q. N. Yin, X. Ou, J. Yin, B. Xu, Y. D. Xia, A. D. Li and Z. G. Liu, *Appl. Phys. Lett.* **105** (2014) 123504.
32. K. Jiang, X. Ou, X. X. Lan, J. Yin, B. Xu, Y. D. Xia, A. D. Li and Z. G. Liu, *Appl. Phys. Lett.* **104** (2014) 263506.
33. W. Lu, C. Y. Wei, K. Jiang, J. Q. Liu, J. X. Lu, P. Han, A. D. Li, Y. D. Xia, B. Xu and J. Yin, *AIP Adv.* **5** (2015) 087158.
34. J. X. Lu, X. Ou, X. X. Lan, Z. Y. Cao, X. J. Liu, W. Lu, C. J. Gong, B. Xu, A. D. Li, Y. D. Xia, J. Yin and Z. G. Liu, *Chin. Phys. Lett.* **31** (2014) 028503.
35. S. Maikap, H. Y. Lee, T. Y. Wang, P. J. Tzeng, C. C. Wang, L. S. Lee, K. C. Liu, J. R. Yang and M. J. Tsai, *Semicond. Sci. Technol.* **22** (2007) 884.
36. S. Maikap, S. Z. Rahaman and T. C. Tien, *Nanotechnology* **19** (2008) 435202.